EXHIBIT 1

PATENT
Attorney Docket No. 8812.0003-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Melvin James BULLEN et al.	Group Art Unit: 2113
Application No.: 11/710,407	Examiner: Michael C. Maskulinski
Filed: February 26, 2007	
For: METHODS AND SYSTEMS FOR A STORAGE SYSTEM	Confirmation No.: 5026

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY TO OFFICE ACTION

In reply to the Office Action mailed March 27, 2008, the date for response to which has been extended to July 27, 2008, by a petition for a one-month extension of time filed concurrently herewith, please see the remarks below:

REMARKS

In this Reply, Applicants have not amended the claims or added any new matter. Claims 1-4, 9-15, 25-27, 31-34, and 40 remain pending.

In the Office Action[1], the Examiner rejects claims 1, 26, and 40 on the grounds of obviousness-type double patenting over claims 1 and 14 of U.S. Patent No. 7,192,662. The Examiner also rejects claims 1-4, 9-15, 25-27, 31-34, and 40 under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,981,173 to Ferguson et al. ("*Ferguson*").

Regarding the obviousness-type nonstatutory double patenting rejection, Applicants attach a terminal disclaimer with this Reply. The terminal disclaimer overcomes the double patenting rejection. Accordingly, Applicants request withdrawal of the double patenting rejection of claims 1, 26, and 40.

Regarding the claim rejections based upon 35 U.S.C. § 102, Applicants traverse these rejections. In order to properly anticipate the rejected claims under 35 U.S.C. § 102(e), *Ferguson* must disclose each and every limitation recited in the claims. (*See* M.P.E.P. § 2131). For at least the reasons detailed below, *Ferguson* fails to disclose all the limitations recited in the claims.

The described system in *Ferguson* contains a host/data controller 16/18 that uses a "4+1" RAID architecture to draw data out from the memory segments 24, pulling a quad-word from four of the memory segments 24A-D and a parity bit from the remaining segment 24E. (Col. 5, lines 56-61; Fig. 2). The data controller then uses the

[1] In the Office Action, the Examiner characterizes the claims and the teachings of the cited references. Applicants decline to subscribe to any of the Examiner's characterizations, whether or not they are specifically mentioned in this Reply.

parity information and error code correction modules 40 to detect and correct any errors in the received data before forwarding it to external devices 32-36. (Col. 6, lines 19-55; Fig. 1). Even when the data controller performs an error correction operation, the data input from any particular memory segment 24 always goes to its corresponding output bus 52. (Fig. 2). The data controller cannot be reconfigured to switch input data to a different output bus 52. For example, data from memory segment 24A input via bus segment 22A to the data controller is always output via output bus 52A; the data controller cannot reconfigure the interconnection to output that data on one of the other output buses 52B-E. (Fig. 2 and related text). Thus, *Ferguson* teaches a nonconfigurable, hardwired interconnection from the memory segments 24 via bus segments 22 to bus 52 connected to external devices 32-36.

The storage system recited in claim 1, in contrast, comprises, among other things, "one or more switches including" "a selectively configurable switch fabric," wherein the "switch fabric [is] connected to one or more memory sections and external device interfaces" and the configurable switch fabric "interconnect[s] the memory sections and the external device interfaces based on an algorithm." In the Office Action, the Examiner asserted that *Ferguson*'s data controller 18 anticipates these claim elements. (OA, pg. 4). This is incorrect because *Ferguson*'s system moves data from the memory segments 24 to an error detection and decoding system within the data controller 18 along a single, hardwired, unchangeable path. (Fig. 2; Col. 5, lines 15-21). This is necessitated by design in *Ferguson*, which uses redundancy among memory segments, requiring them to act in lock-step cooperation with one another instead of acting independently (as stated at col. 4, lines 65-66) and thus does not allow them to

have selectively configurable interconnections to external devices. Thus, *Ferguson* does not teach or suggest "a selectively configurable switch fabric" having the features expressly recited in claim 1.

Ferguson also fails to teach or suggest other elements of claim 1. In part 4, subsection d on pages 4-5 of the Office Action, the Examiner asserts the *Ferguson* patent anticipates the portion of claim 1 reciting, "a management system capable of receiving fault messages from the memory section controllers and inactivating the memory section corresponding to the fault message received, and wherein the management system is further capable of determining the algorithm for use by the selectively configurable switch fabric in interconnecting the memory sections and the one or more interfaces, and controlling the one or more switches to execute the determined algorithm" because *Ferguson* discloses memory segments each having an associated control mechanism in the data controller 18 which facilitates the power up and power down procedures, where the power down state is implemented when a memory cartridge is being replaced. (Col. 7, lines 12-15; col. 7, lines 64-66). Contrary to the examiner's assertions, *Ferguson's* control mechanism does not teach these claimed features, among others.

Ferguson's control mechanism interprets, "the independent transitioning of each memory cartridge between various states." (Abstract, claim 1). Each memory segment has an associated control mechanism in the data controller which is configured to facilitate the power up and power down procedures for each bus segment. (Col. 7, lines 12-15). State control is not dictated by the control mechanism, but by the host/data controller or CPU. (Col. 7, lines 23-24). A control mechanism merely interprets

transitions between the various states based on software commands implemented by the data controller and dependent on the system state. (Col. 9, lines 9-13). The control mechanism is apparently used to provide current state information in the data controller, and plays a role in "hot-plugging" a memory cartridge. (Col. 7, lines 27-28; Col. 8, lines 2-4; Abstract).

In contrast, the management system of claim 1 can 1) receive fault messages from the memory section controllers, 2) determine the algorithm for use by the selectively configurable switch fabric in interconnecting the memory sections and the interfaces, and 3) control the one or more switches to execute the determined algorithm, among other things. Contrary to the Examiner's assertions, the *Ferguson* control mechanism does not receive fault messages from the memory section controller. *Ferguson* teaches that the control mechanism interprets the change of state, facilitates the power up and power down procedures of the bus to a memory section, monitors the state of a memory bus and provides current state information to the data controller. (Claim 1; Abstract; Col. 7, lines 13-15; Col. 8, lines 2-7; Col. 9, lines 9-12). Nowhere in the *Ferguson* reference does it teach or suggest that the control mechanism receives fault messages.

Ferguson's control mechanism 58 does not "determin[e] the algorithm for use by the selectively configurable switch fabric in interconnecting the memory sections and the external devices," and "control[] the one or more switches to execute the determined algorithm," as the Examiner asserted in the Office Action (pg. 4-5) because, as explained above, *Ferguson*'s data controller 18 does not function as a switch that includes "a selectively configurable switch fabric .... [that] interconnect[s] the memory

sections and external device interfaces," as recited in claim 1. Consequently, the control mechanism 58 does not determine an algorithm for use by the data controller 18 because the data controller is not selectively configurable. Control mechanism 58 does not and cannot instruct the data controller 18 to execute any algorithm at all. Even assuming, *arguendo*, that *Ferguson*'s control mechanism 58 is used for powering the memory segments up and down and running through various states which can restore data to a memory segment which has been removed and replaced, as the Examiner asserts (OA, pgs. 3-4), *Ferguson*'s control mechanism 58 and controller-ordered state changes do not change the interconnection between external devices 32-36 and memory segments 24 based on an algorithm, and thus do not teach or suggest the features recited in claim 1.

Thus, for at least the foregoing reasons, *Ferguson* does not disclose each and every element recited in independent claim 1. Accordingly, Applicants respectfully submit that claim 1 is allowable over *Ferguson*. Furthermore, for at least the same reasons, independent claims 26 and 40, although of different scope, are also not anticipated by *Ferguson*. In addition, dependent claims 2-4, 9-15, 25, 27, and 31-34 are also allowable over *Ferguson*, at least by virtue of their dependence from allowable independent claims 1, 26 and 40, respectively.

Ferguson also does not support a prima facie case of anticipation of the claims for another reason--*Ferguson's* control mechanism disclosure does not meet the anticipatory enablement requirement. In *Paulsen*, the Federal Circuit held that a rejection for anticipation under 35 U.S.C. §102 requires that, "the reference must be enabling and describe the applicant's claimed invention sufficiently to have placed it in

possession of a person of ordinary skill in the field of the invention." (*In re Paulsen*, 30 F.3d 1475 (Fed. Cir. 1994); also see M.P.E.P. § 2121.01). *Ferguson* merely uses words such as "facilitates" and "interprets" to describe the control mechanism's functions, providing no details as to how it performs the functions and no information regarding the control mechanism's structure. Indeed, the only drawing which includes a control mechanism is figure 2, in which the control mechanism is shown as a featureless box that is not connected to anything. *Ferguson*'s teaching of an unconnected, black-box control mechanism does not enable one of skill in the art to understand how the control mechanism could determine the algorithm for use by the selectively configurable switch fabric in interconnecting the memory sections and the interfaces or control the one or more switches to execute the determined algorithm, among other things recited in the claims.

Thus, for at least this additional reason, *Ferguson* does not support a prima facie case of anticipation of the independent claims. Accordingly, Applicants respectfully submit that claims 1, 26 and 40 are allowable over *Ferguson*. In addition, dependent claims 2-4, 9-15, 25, 27, and 31-34 are also allowable over *Ferguson*, at least by virtue of their dependence from allowable independent claims 1, 26 and 40, respectively.

In view of the foregoing remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 18, 2008

By: William J. Brogan
William J. Brogan
Reg. No. 43,515

EXHIBIT 2

PATENT
Attorney Docket No. 08812.0003-01000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Melvin James BULLEN et al.	)	Group Art Unit: 2113
	)	
Application No.: 11/710,407	)	Examiner: Michael C. Maskulinski
	)	
Filed: February 26, 2007	)	
	)	
For: METHODS AND SYSTEMS FOR A STORAGE SYSTEM	)	Confirmation No.: 5026
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY TO OFFICE ACTION

In reply to the Final Office Action mailed October 23, 2008, the date for reply being extended to February 23, 2009, by a petition for one month extension of time filed herewith, and pursuant to 37 C.F.R. § 1.116, Applicants file concurrently herewith a Request for Continued Examination (RCE) and amend this application pursuant to 37 C.F.R. § 1.114 as follows:

Amendments to the Claims are reflected in the listing of claims in this paper.

Remarks follow the amendments section of this paper.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A storage system, comprising:

one or more memory sections, including:

one or more memory devices having storage locations for storing data, and

a memory section controller capable of detecting faults in the memory section and transmitting a fault message in response to the detected faults; ~~and~~

one or more switches, including:

one or more interfaces for connecting to one or more external devices;

a switch controller that executes software, including a routing algorithm; and

a selectively configurable switch fabric connected to one or more memory sections and the one or more interfaces and interconnecting the memory sections and the one or more interfaces based on the routing ~~an~~ algorithm stored in the switch controller; and

a management system capable of receiving fault messages from the memory section controllers and inactivating the memory section corresponding to the fault message received by changing the routing algorithm, and wherein the management system is further capable of determining and changing the routing algorithm for use by the selectively configurable switch fabric in interconnecting the memory sections and the one or more interfaces, providing the determined routing algorithm to the switch

controller, and ~~controlling the one or more switches~~ instructing the switch controller to execute the determined routing algorithm.

2. (Currently Amended) The storage system of claim 1, wherein the one or more switches further include:

one or more memory section interfaces for connecting the one or more switches with the memory sections, such that the selectively configurable switch fabric is connected to the memory sections via the memory section interfaces~~;~~

~~a switch controller for receiving the instruction from the management system and executing the algorithm~~.

3. (Previously Presented) The storage system of claim 1, wherein the management system controls the selectively configurable switch fabric and the one or more interfaces.

4. (Previously Presented) The storage system of claim 2, wherein the management system is further capable of providing software images to the switch controllers and to the memory section controllers.

5.-8. Cancelled.

9. (Previously Presented) The storage system of claim 1, wherein the storage locations of the one or more memory devices are partitioned into at least one

block, the block identifiable by a block identifier, and wherein a data request received by the storage system includes a block identifier; and wherein a switch receiving the data request directs the data request to a memory section including the block identified by the block identifier; and wherein the memory section reads data stored in at least one storage location of the one or more memory devices identified by the block identifier and forwards the read data to a destination device via the one or more switches.

10. (Previously Presented) The storage system of claim 1, wherein a plurality of parallel lines connect at least one of the memory sections to a switch, and wherein data from the memory section is passed through the selectively configurable switch fabric of the switch in parallel.

11. (Previously Presented) The storage system of claim 10, wherein at least a portion of the data passed through the selectively configurable switch fabric in parallel is synchronously passed through the selectively configurable switch fabric.

12. (Previously Presented) The storage system of claim 1, wherein a plurality of parallel lines connect at least one of the memory sections to a switch, further comprising:

one or more multiplexers for multiplexing signals through the parallel lines.

13. (Original) The storage system of claim 12, wherein at least one multiplexer is included in one of the switches.

14. (Previously Presented) The storage system of claim 1, wherein at least one memory section may be added or removed from the storage system.

15. (Original) The storage system of claim 1, wherein the management system is further capable of bringing into service memory sections added to the storage system.

16.-24. Cancelled.

25. (Original) The storage system of claim 1, wherein at least one memory section further includes at least one communications channel interface for receiving data to be stored by the memory section and transferring the data to be stored to one or more of the memory devices, and wherein the communications channel interface is further capable of receiving data read from the memory devices and transferring the data read from the memory devices to one or more of the switches, and wherein the communications channel interface is further capable of receiving data requests and forwarding the data requests to the memory section controller.

26. (Currently Amended) A method for use in a storage system, comprising:

storing data in a storage locations in a memory device, the memory device included in a memory section;

a management system determining a ~~an~~ routing algorithm for use by a switch controller that executes software, including the routing algorithm, to configure a selectively configurable switch in connecting the memory section and an interface;

the management system providing the determined routing algorithm to the switch controller and instructing the switch controller to execute the determined routing algorithm;

the selectively configurable switch connecting the memory section to the interface based on the routing algorithm;

detecting by a memory section controller a fault in regard to the data stored in the memory device and transmitting a fault message in response to the detected fault to the management system;

receiving the fault message at the management system; and

the management system removing from service the memory section from which the fault message was received by changing the routing algorithm.

27. (Previously Presented) The method of claim 26, further comprising:

the management system providing a software image to the selectively configurable switch; and

the management system providing a software image to the memory section controller.

28.-30. Cancelled.

31. (Previously Presented) The method of claim 26, wherein the storage locations of the memory devices are partitioned into data blocks, the data blocks identifiable by a data block identifier, and wherein a data request received by the storage system includes a data block identifier, further comprising:

the selectively configurable switch directing the data request to a memory section including the memory device storing the data block identified by the data block identifier;

the memory section reading from the memory device data stored in the storage locations of the memory devices identified by the data block identifier; and

forwarding the read data to a destination device via the selectively configurable switch.

32. (Previously Presented) The method of claim 26, wherein a plurality of parallel lines connect the memory section to the selectively configurable switch, further comprising passing data from the memory section through the selectively configurable switch in parallel.

33. (Previously Presented) The method of claim 26, further comprising:

connecting a new memory section to the selectively configurable switch during a portion of a first period during which data is being read from the memory device; and

disconnecting a memory section from the selectively configurable switch during a portion of a second period during which data is being read from the memory device.

34. (Previously Presented) The method of claim 26, further comprising:

the management system bringing into service memory sections connected to the selectively configurable switch.

35.-39. Cancelled.

40. (Currently Amended) A storage system comprising:

means for storing, including:

means for storing data in storage locations; and

means for detecting a fault in regard to the data stored by the means for storing and transmitting a fault message in response to the detected fault;

programmable means for switching data being transmitted between the means for storing and one or more interfaces based on a routing algorithm; and

means for receiving the fault message, removing from service the means for storing from which the fault message was received by changing the routing algorithm, determining ~~an~~ the routing algorithm for use by the programmable means for switching in connecting the means for storing and the one or more interfaces, and instructing the programmable means for switching to execute the determined routing algorithm, such that the programmable means for switching connects the means for storing to the one or more interfaces based on the routing algorithm.

REMARKS

Applicants file concurrently herewith a Request for Continued Examination (RCE) in response to the Final Office Action mailed October 23, 2008 (hereinafter, "Office Action"). In the Office Action[1], the Examiner rejected claims 1-4, 9-15, 25-27, 31-34, and 40 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,981,173 to Ferguson et al. ("*Ferguson*").

By this response, Applicants hereby amend claims 1, 2, 26, and 40. The amendments to the claims are supported by the specification, see paragraphs [0066], [0067], [0087], [0092] - [0095], [0113], [0114], [0115], Fig. 6, and Fig. 8, among other places. Claims 5-8, 16-24, 28-30, and 35-39 were previously canceled. Accordingly, upon entry of this Amendment, claims 1-4, 9-15, 25-27, 31-34, and 40 remain pending.

In light of the foregoing amendments and based on the reasoning presented below, Applicants respectfully traverse the rejection of the pending claims under 35 U.S.C. § 102(e), and request allowance of claims 1-4, 9-15, 25-27, 31-34, and 40.

I. Claim Rejection Under 35 U.S.C. § 102(e)

Regarding the claim rejections based upon 35 U.S.C. § 102, Applicants traverse these rejections. In order to properly anticipate the rejected claims under 35 U.S.C. § 102(e), *Ferguson* must disclose each and every limitation recited in the claims. (*See* M.P.E.P. § 2131). For at least the reasons detailed below, *Ferguson* fails to disclose all the limitations recited in the claims.

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[1] In the Office Action, the Examiner characterizes the claims and the teachings of the cited references. Applicants decline to subscribe to any of the Examiner's characterizations, whether or not they are specifically mentioned in this Reply.

For example, amended claim 1 recites "a switch controller that executes software, including a routing algorithm" and "a management system capable of ... determining and changing the routing algorithm for use by the selectively configurable switch fabric in interconnecting the memory sections and the one or more interfaces, providing the determined routing algorithm to the switch controller, and instructing the switch controller to execute the determined routing algorithm." (Amended claim 1, emphasis added).

The system described in *Ferguson* contains a control mechanism 58A-58E associated with each memory segment 24A-24E. (Col. 7, lines 12-14). Each control mechanism 58A-58E "is configured to facilitate the power up and power down procedures associated with each bus segment 22A-22E." (Col. 7, lines 13-15). "The control mechanisms 58A-58E are used to provide the current state information in the data controller." (Col. 7, lines 27-29). The Examiner characterizes *Ferguson* as disclosing "a control mechanism in the data controller which is configured to facilitate the power up and powerdown procedures associated with each bus segment (a switch controller for receiving the instruction from the management system and executing the algorithm)." (Office Action, page 4). While control mechanism 58A-58E may be configured to facilitate the power up and powerdown procedures associated with each bus segment, control mechanisms 58A-58E are not "a switch controller that executes software, including a routing algorithm" because control mechanism 58A-58E does not execute software, does not execute a routing algorithm, and does not control multiplexers 44A-44E. (Col. 7, lines 27-32; Col. 8, lines 2-7). Control mechanisms 58A-58E "are used to provide the current state information in the data controller 18." (Col. 7,

lines 27-29). Providing state information is neither executing software, executing a routing algorithm, nor controlling switches.

Moreover, *Ferguson's* control mechanism 58 is not provided with a "routing algorithm" that is determined or changed by "a management system." Similarly, *Ferguson's* control mechanism 58 cannot be instructed "to execute the determined routing algorithm," as recited in amended claim 1. In sum, *Ferguson* does not teach or suggest a switch controller having the features recited in claim 1.

Furthermore, *Ferguson's* host data controller 18 does not teach or suggest "interconnecting the memory sections and the one or more interfaces based on the routing algorithm stored in the switch controller" because, as explained above, *Ferguson's* system does not include a switch controller, as recited in amended claim 1.

Additionally, amended claim 1 recites "a management system capable of receiving fault messages from the memory section controllers and inactivating the memory section corresponding to the fault message received by changing the routing algorithm." (Amended claim 1, emphasis added). *Ferguson* fails to disclose this feature because *Ferguson* teaches a hardwired system. Even assuming, arguendo, that *Ferguson's* error detectors and muxes implement an algorithm, as the Office Action asserts, (and as Applicants disagree), a hardwired algorithm cannot be changed, as recited in claim 1. Thus, *Ferguson* does not teach or disclose "a management system capable of receiving fault messages from the memory section controllers and inactivating the memory section corresponding to the fault message received by changing the routing algorithm." (Amended claim 1, emphasis added).

Thus, for at least the foregoing reasons, *Ferguson* does not disclose each and every element recited in amended independent claim 1. Accordingly, Applicants respectfully submit that claim 1 is allowable over *Ferguson*. Furthermore, for at least the same reasons, independent claims 26 and 40, although of different scope, are also not anticipated by *Ferguson*.

In addition, dependent claims 2-4, 9-15, 25, 27, and 31-34 are also allowable over *Ferguson*, at least by virtue of their dependence from allowable independent claims 1 and 26 respectively. Dependant claims 2-4, 9-15, 25, 27, and 31-34 are also allowable because they recite additional features not taught or suggested by the cited reference.

For example, dependant claim 4 recites "the management system is further capable of providing software images to the switch controllers and to the memory section controllers." (Claim 4, emphasis added). The Examiner states that *Ferguson* "discloses that the control mechanism may interpret transitions between the various states based on the software commands implemented by the data controller and dependant on the particular state of the system." (Office Action, page 4). A software image is commonly understood as a binary object code that may be run directly by a computer. (Specification, paragraph [0069]). *Ferguson* does not suggest or teach "providing software images to the switch controllers and to the memory section controllers" because *Ferguson's* control mechanism 58 and data controller 18 do not contain a computer that could execute or be provided with a software image. (Claim 4, emphasis added).

Thus, for at least this additional reason, *Ferguson* does not support a case of anticipation of dependent claim 4. Furthermore, for at least the same reasons, dependent claim 27, although of different scope, is also not anticipated by *Ferguson*.

II. Information Disclosure Statement (IDS) of July 18, 2008

Applicants note that the Examiner did not return an initialed copy of the PTO/SB/08 Form filed with the Information Disclosure Statement (IDS) of July 18, 2008. For the Examiner's convenience, Applicants include a copy of the PTO/SB/08 Form that was attached to the IDS. Applicants request that the Examiner consider the listed documents and return the Form including appropriate notations indicating the Examiner's consideration.

Additionally, Applicants include a new IDS with a PTO/SB/08 Form attached. Applicants request that the Examiner consider the listed documents and return the Form including appropriate notations indicating the Examiner's consideration.

II. Conclusion

In view of the foregoing remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 23, 2009

By: _____
Daniel R. Lupo
Reg. No. 59,269

ATTACHMENT: Copy of PTO/SB/08 filed July 18, 2008

EXHIBIT 3

PATENT
Customer No. 22,852
Attorney Docket No. 08812.0004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
M. James Bullen et al.	Group Art Unit: 2187
Application No.: 10/284,278	Examiner: Christian Chace
Filed: October 31, 2002	
For: Methods and Systems for a Storage System Including an Improved Switch	Confirmation No.: 8809

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY TO OFFICE ACTION

In reply to the Office Action mailed March 18, 2005, the period for response to which extends through July 18, 2005, with a one-month extension, please amend the above-identified application as follows:

Amendments to the Specification are included in this paper.

Remarks/Arguments follow the amendment section of this paper.

AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows:

Please replace the title with the following new title:

METHODS AND SYSTEMS FOR A STORAGE SYSTEM WITH A PROGRAM-CONTROLLED SWITCH FOR ROUTING DATA

On page 2 of the application, please replace paragraph [0002] with the following replacement paragraph:

[0002] The present application relates to the U.S. Patent Application Serial No.: [[____]] 10/284,199 by M. James Bullen, Steven L. Dodd, David J. Herbison, and William T. Lynch, entitled "Methods and Systems for a Storage System," Attorney Docket No.: 08812-0003, and the U.S. Patent Application Serial No.: [[____]] 10/284,268 by M. James Bullen, Steven L. Dodd, David J. Herbison, and William T. Lynch, entitled "Methods and Systems for a Memory Section," Attorney Docket No.: 08812-0005, both of which are incorporated by reference herein in their entireties.

On page 41 of the application, please replace paragraph [0119] with the following replacement paragraph:

[0119] The memory interface device 64 may also receive control and timing signals from the timing circuitry 61 of the section controller 54. These control and timing pulses may be timed such that the data read from or written into a memory device 66 using the respective pulses are read or written in such a manner that the shift registers 76 of the memory interface device maintain their shifting as if only a shift was taking

place. For a further description of memory interface devices incorporating shift registers, please see ~~the aforementioned~~ U.S. Patent Application Serial No. [[____]] 10/284,198 by William T. Lynch and David J. Herbison, entitled "Methods and Apparatus for Improved Memory Access," (issued as U.S. Patent No. 6,879,526) which [[was]] is incorporated by reference herein in its entirety. Additionally, data transmitted by a memory interface device 64 may, for example, be transmitted in common mode, differential mode, or in any other manner as deemed appropriate by the system designers.

On pages 45-46 of the application, please replace paragraph [0129] with the following replacement paragraph:

[0129] A more detailed description of the connections between the shift register arrays and the memory devices and a method for writing the data is presented in the aforementioned U.S. Patent Application Serial No.:[[____]] 10/284,198 by William T. Lynch and David J. Herbison entitled "Methods and Apparatus [[of]] for Improved Memory Access" (issued as U.S. Patent No. 6,879,526) filed on the same day as the present application.

On pages 61-62 of the application, please replace paragraph [0166] with the following replacement paragraph:

[0166] As will be obvious to one of skill in the art, other embodiments of the memory interface device are possible, without departing from the scope of the invention. For example, although each memory interface device is described as only having one

read or write shift register array, the memory interface device may include any number of write or read chains of shift register arrays. Further, the shift registers 76 rather than being 1 bit shift registers may be of any depth. For example, the shift register arrays could be, for example, NxM arrays such as, for example, 2x8, 4x32, 8x16, etc. arrays as determined by the system designers for their particular implementation. Additionally, the shift registers arrays may be configured in a ring, such that the data once loaded into a chain circulates synchronously in the chain. A more detailed description of memory access using shift register arrays is set forth in the aforementioned U.S. Patent Application Serial No. [[____]] 10/284,198 by William T. Lynch and David J. Herbison entitled "Methods and Apparatus for Improved Memory Access" (issued as U.S. Patent No. 6,879,526) filed on the same day as the present application.

REMARKS

As a preliminary matter, Applicants note that the Examiner did not include an initialed copy of the form PTO/SB/08 filed by Applicants with an IDS on March 7, 2005. Applicants request that the Examiner provide an initialed copy at the Examiner's earliest opportunity. For the Examiner's convenience, Applicants have enclosed another copy of the IDS and form PTO/SB/08 filed on March 7, 2005.

In this Reply, Applicants have amended the title and specification of the application. Claims 1-26 remain pending.

Summary

In the Office Action, the Examiner objected to the attempt to incorporate subject matter by reference because the serial numbers of the related applications were missing from the specification. In addition, the Examiner provisionally rejected claims 1, 2, 7, and 12-16 under the doctrine of obviousness-type double patenting in view of copending U.S. Application No. 10/284,268; rejected claims 12 and 13 under the doctrine of obviousness-type double patenting in view of U.S. Patent No. 6,879,526; rejected claim 26 under 35 U.S.C. § 112, second paragraph as being indefinite; rejected claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4, 796,231 to *Pinkham*; and rejected claims 3-7 and 18-20 under 35 U.S.C. § 103(a) as being unpatentable over *Pinkham* in view of the Examiner's official notice of memory fault detection and recovery techniques allegedly known in the art. Applicants traverse these objections and rejections for the reasons given below.

Objections

In the Office Action, the Examiner objected to the attempt to incorporate the subject matter or related applications by reference because the serial numbers of the related applications were unknown at the time of filing and therefore missing from the specification. Applicants have amended the specification to insert the serial numbers. Applicants accordingly request the withdrawal of this objection. The Examiner also objected to the title as not descriptive. Applicants have provided a new descriptive title and request the withdrawal of this objection.

Double Patenting Rejections

In the Office Action, the Examiner provisionally rejected claims 1, 2, 7, and 12-16 under the doctrine of obviousness-type double patenting in view of copending U.S. Application No. 10/284,268. In accordance with M.P.E.P. §§ 804 and 1490, and without admitting or even agreeing with the Examiner's allegations of anticipation and double patenting, and while reserving the right to traverse the Examiner's allegations of anticipation or double patenting in the future, Applicants defer responding to the provisional double patenting rejection until it is the only rejection remaining in the two applications, and the Examiner withdraws the provisional double-patenting rejection as to one application and permits that application to issue as a patent, thereby converting the provisional double patenting rejection in the other application into a double patenting rejection at the time the other application issues as a patent.

In the Office Action, the Examiner rejected claims 12 and 13 under the doctrine of obviousness-type double patenting in view of U.S. Patent No. 6,879,526, which recently issued from U.S. Application No. 10/284,198. In reply, and without admitting or even agreeing with the Examiner's allegations of anticipation and double patenting, and

while reserving the right to traverse the Examiner's allegations of anticipation or double patenting in the future, Applicants file herewith a terminal disclaimer in compliance with 37 C.F.R. 1.321(c) to overcome the rejection of claims 12 and 13 under the doctrine of obviousness-type double patenting. Accordingly, claims 12 and 13 are in condition for allowance, and Applicants request the withdrawal of the double patenting rejection of those claims.

35 U.S.C. § 112 Rejections

In the Office Action, the Examiner rejected claim 26 under 35 U.S.C. § 112, second paragraph as being indefinite because it is allegedly unclear what means in the specification correspond to the means recited in claim 26. The Examiner required that the Applicants particularly, clearly, and distinctly point out what means claim 26 refers to.

In claim 26, the "means for storing" refers to at least a memory section structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7 and 16 and related text. The "means for storing data in storage locations" refers to at least a memory device structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7 and 14 and related text. The "means for controlling the means for storing" refers to at least a memory section controller structure and a section controller structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7 and related text. The "means for mapping" refers to at least a memory section controller structure, a section controller structure, a resident memory structure, an internal controller memory, and a control processor, and components and

equivalents thereof, described in the specification in, among other places, Figures 4-7 and related text. The "means for providing the addresses" refers to at least a memory section controller structure, a section controller structure, a memory device control circuitry, and a memory latch structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 12 and related text. The "means for switching" refers to at least a switch structure and components and equivalents thereof, described in the specification in, among other places, Figures 2 and 6-9 and related text. The "means for receiving a data request" refers to at least a switch structure and a switch server communications interface structure, and components and equivalents thereof, described in the specification in, among other places, Figures 6-9 and related text. The "means for switching the data request" refers to at least a switch fabric structure, and a switch controller structure, and components and equivalents thereof, described in the specification in, among other places, Figures 6-9 and related text. And, the "means for forwarding" refers to at least a switch memory section interface structure and a switch fabric structure, and components and equivalents thereof, described in the specification in, among other places, Figures 6-9 and related text.

Applicants have particularly, clearly, and distinctly pointed out structures that claim 26 refers to. Accordingly, claim 26 is in condition for allowance, and Applicants request the withdrawal of the 35 U.S.C. § 112, second paragraph, rejection.

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4, 796,231 to Pinkham

("*Pinkham*"). The Examiner also incidentally alleged that U.S. Patent No. 4,510,599 to *Ulug* ("*Ulug*") and U.S. Patent No. 6,728,799 to Perner et al. ("*Perner*") also anticipate claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b), but did not rely on *Ulug* or *Perner* et al. as a specific basis for rejection. Applicants traverse the rejection of claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b).

In order to properly anticipate claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(a), *Pinkham* must explicitly disclose each and every limitation recited in the claims. *See* M.P.E.P. § 2131 (7th ed. 1998). If *Pinkham*, however, fails to expressly set forth a particular limitation, then the Examiner must show that this limitation is inherently disclosed to substantiate a claim of anticipation. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). To establish inherency, the Examiner must specifically identify extrinsic evidence that makes clear to one skilled in the art that the missing limitation "is necessarily present" in the *Pinkham* disclosure. *See id.; see also Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1269 (Fed. Cir. 1991).

Pinkham does not disclose each and every limitation recited in the claims. In general, the Office Action does not address, analyze, or compare to *Pinkham* every limitation recited in the claims. Instead, the Office Action attempts to merely match the names of components recited in the claims with similarly named components disclosed in *Pinkham*, while improperly ignoring the functions, connections, and interactions of the components and operations expressly recited in the claims.

For example, independent claim 1 recites, among other things, "one or more switches for receiving a data request including a data block identifier and switching the

data request based on the data block identifier to one or more of the memory sections, the data block identifier identifying a set of storage locations."

Pinkham does not teach or suggest switches with the features and functions recited in claim 1. Although *Pinkham* discloses single pole double throw switches, the switches in *Pinkham* are not at all like those recited in claim 1. The switch is *Pinkham* is an "A/B switch" (56, 58, 60, 62) that merely directs the output of a tap latch (42, 44, 46, 48) to either: A) the input of the shift register being tapped as a circulating shift register, or B) the input of another cascaded shift register. (Col. 5, line 42 - col. 6, line 54; Fig. 1). *Pinkham*'s switches do not perform any of the functions of the switches recited in claim 1. *Pinkham*'s switches do not receive a data request including a data block identifier as recited in claim 1. They do not receive anything. The switches in *Pinkham* are used to configure shift register output connections; they are merely single pole double throw switches that switch the shift registers between circulating and cascade mode based on whether they are thrown to one circuit path or the other. Similarly, *Pinkham*'s switches do not switch the data request based on the data block identifier to one or more of the memory sections as recited in claim 1. The single pole double throw switches of *Pinkham* simply do not have the capability to operate based on a block identifier or to direct a data request. Furthermore, nothing else disclosed in *Pinkham* (or *Ulug* or *Pemer*) performs these functions.

For at least the foregoing reasons, *Pinkham* fails to disclose each and every element recited in independent claim 1, and therefore claim 1 is allowable over *Pinkham*. Similarly, independent claims 16 and 26, which recite features similar to those recited in claim 1, are also allowable for at least the same reasons. In addition,

dependent claims 2-15 and 17-25 are allowable at least by reason of their dependence from allowable independent claims 1 and 16 respectively. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Regarding claim 2, *Pinkham* does not teach or suggest a management system as recited in claim 2. Specifically, claim 2 recites the storage system of claim 1, further comprising a management system for providing an algorithm to at least one of the one or more switches, wherein the switch executes the algorithm in switching the data request based on the data block identifier. First, as explained above, *Pinkham* teaches only conventional single pole double throw switches that are not capable of "execut[ing] the algorithm in switching the data request based on the data block identifier" as recited in claim 2. Moreover, in the Office Action, the Examiner asserts that the "two modes of operation of the shift registers," (i.e., throwing an A/B switch to change the output circuit of the shift registers from a circulating connection to a cascade connection), disclose "a management system for providing an algorithm to at least one of the one or more switches," but there is no concept of a management system in *Pinkham* that Applicants can discern. *Pinkham's* signal to throw an A/B switch is not an algorithm. Nor does *Pinkham* disclose what throws the A/B switches or how they are switched, as far as Applicants can discern. Consequently, *Pinkham* contains no concept of control or management of the switches or of "providing an algorithm to at least one of the one or more switches" as recited in claim 2. *Ulug* and *Perner* similarly lack any teachings or suggestions related to a management system as recited in claim 2.

For at least this additional reason, *Pinkham* fails to disclose each and every element recited in claim 2, and claim 2 is allowable over *Pinkham*. Similarly, claim 17, which recites features similar to those recited in claim 2, is also allowable for at least the same additional reason. In addition, dependent claims 3-6 and 18-20 are allowable at least by reason of their dependence from allowable claims 2 and 17 respectively. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Regarding claims 12, 13, 23, and 24, *Pinkham* does not teach or suggest each and every element recited. For example, claim 12 recites, among other things, "wherein data from one or more of the output of a memory device is loaded into a corresponding shift register in the sets of shift registers and the loaded data is shifted from the shift register to a next one of the shift registers in the set according to the shift frequency, such that the shift register maintains its shift frequency during any loading of the data." *Pinkham* does not teach or suggest anything related to the concept that the shift register maintains its shift frequency during any loading of the data. Nor does the Examiner assert as much. In the Office Action, the Examiner extrapolates that the clock-driven cascaded mode of operation discloses that "the clock signal received by the shift register maintains its shift frequency during any loading of the data." But this is not what claim 12 recites. Claim 12 recites "that the shift register maintains its shift frequency during any loading of the data," not that the clock signal maintains its shift frequency. *Pinkham*, in fact, lacks any teaching or suggestion related to a shift register maintaining its shift frequency while at the same time loading data, as do *Ulug* and *Perner*.

For at least this additional reason, *Pinkham* fails to disclose each and every element recited in claim 12, and therefore claim 12 is allowable over *Pinkham*. Similarly, claims 13, 23, and 24, which recites features similar to those recited in claim 12, are also allowable for at least the same additional reason. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Regarding claims 9, 10, and 22, *Pinkham* does not teach or suggest anything related to "an identifier for use in forwarding the requested data," as recited in claim 9. *Pinkham* is silent regarding where data goes after being read out of a memory device and how it is forwarded to another device. *Ulug* and *Pemer* similarly lack any teachings or suggestions related to an identifier for use in forwarding the requested data.

For at least this additional reason, *Pinkham* fails to disclose each and every element recited in claim 9, and therefore claim 9 is allowable over *Pinkham*. Similarly, claims 10 and 22, which recites features similar to those recited in claim 9, are also allowable for at least the same additional reason. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 3-7 and 18-20 under 35 U.S.C. § 103(a) as being unpatentable over *Pinkham* in view of the Examiner's official notice of memory fault detection and recovery techniques allegedly known in the art. Applicants traverse.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, the Examiner must demonstrate that (1) *Pinkham* and the officially noticed techniques

disclose or suggest each and every limitation recited in the claims; (2) there is a reasonable probability of success of any modification of the teachings of *Pinkham*, and (3) there exists some suggestion or motivation, either in the teachings of *Pinkham* itself or in the knowledge generally available to one of ordinary skill in the art, to make such a modification in a manner resulting in the claimed invention. *See* M.P.E.P. § 2143 (7th ed. 1998). Furthermore, each of these requirements must be found in the prior art -- not based on Applicants' own disclosure. *See id.*

For the reasons detailed above, *Pinkham* fails to teach or suggest several elements recited in claims 1, 2, 16, and 17, from which claims 3-7 and 18-20 depend. Even assuming, *arguendo*, that the Examiner's official notice of memory fault detection and recovery techniques allegedly known in the art is accurate, the official notice fails to teach or suggest the missing elements recited in claims 1, 2, 16, and 17. Accordingly, because *Pinkham* combined with the Examiner's official notice fails to disclose each and every element recited in the base claims, dependent claims 3-7 and 18-20 are allowable at least by virtue of their dependence from allowable claims 1, 2, 16, and 17.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 7, 2005

By: William J. Brogan
William J. Brogan
Reg. No. 43,515

EXHIBIT 4

W. P. THOMPSON & Co

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• EUROPEAN PATENT ATTORNEYS • CHARTERED PATENT ATTORNEYS •
• EUROPEAN TRADE MARK ATTORNEYS • REGISTERED TRADE MARK AGENTS •

Coopers Building, Church Street, Liverpool, L1 3AB
TELEPHONE: 0151 709 3961 FACSIMILE: 0151 709 0182/0151 708 8602
EMAIL: liverpool@wpt.co.uk WEBSITE: www.wpt.co.uk

August 13, 2008

ElectronicTransmission

EUROPEAN PATENT OFFICE
D-80298 Munich
GERMANY

Dear Sirs,

Re: European Patent Application 03777844.6
RING TECHNOLOGY ENTERPRISES, INC.
Our Ref: RJB/JH/P413744EP

In response to the Communication pursuant to Article 94 (3) EPC dated 11th February 2008, I note first of all that the deadline has been extended to a total of six months, so that taking account of the postal rules this response arrives in good time. To address the objections I file herewith an amended set of claims in full along with amended pages 3, 4, 5, 10, 12, 15, 16, 24, 27, 31, 37, 39 and 64 of the specific description.

To enable the amendments to the claims to be immediately identified, I enclose a "track changes" copy of the claims, with deletions struck through and insertions underlined. So far as the specific description is concerned, I attach photocopies of my working versions showing the current amendments in manuscript.

In section 2.1 of the Communication, the Examiner objects to the language "determining an algorithm" and "based on an algorithm" in claims 1 and 6. The Examiner asserts that the word "algorithm" is not defined, the specific problem solved by the algorithm is not indicated, and subsequently there is an ambiguous link between the algorithm and removing faulty memory sections from service.

As disclosed in the specification in paragraphs 068, 088, 093-4, and 117, among other places, the algorithm is a routing algorithm for determining the interconnection between a memory section (e.g., memory section 30) and an external device interface (e.g., interface 204).

Furthermore the role of the routing algorithm is explained in more detail in the amended independent claims, as will be apparent from review of the "track changes" versions. As to basis for this additional detail, please see below.

Cont/d.....

With reference to section 2.2. of your Communication, please note that page 64 has been amended to remove reference to the "spirit" of the invention. Some of the relevant text has been retained, indicating that the preferred embodiments are presented by way of example and that changes and modifications can be made, with the scope of the invention being indicated by the claims. This, I trust, is acceptable under European practice.

Concerning the features introduced into claim 1, please note the following.

References to the provision and to aspects of the function of the switch controller have been introduced to claims 1 and 6.

As the specification teaches, the switch controller executes software that may be provided by the management system.

> The control processors 34 may also provide the memory sections 30, the switch controller(s) 202, and the I/O Controllers 24 with updated and new software. For example, if software used by the memory sections 30 or the switches 22 become corrupted and/or fails, the control processors 34 can load backup copies of current or previous versions of a software image from its storage 38. Para. 064; see also para. 10.

The software executed by the switch controller includes a routing algorithm, among other things. Abstract; paras. 67; 88; 110. The routing algorithm allows the switch 22 to direct data flowing through the switch according to information contained in the data.

> The switch 22 then may use the data block identifier (DBI) to direct the data request to the memory section 30 that is to store the data block by, for example, determining, based on the DBI, an address for the memory section that the switch 22 uses to route the data request to the memory section (Step 1204). For example, when a data request arrives at an SSCI 204 of a switch 22, the SSCI may, for example, direct the data request to the switch controller 202, which may then, use a table to look up the address corresponding to the DBI, use an algorithm to compute the address from the DBI, or use some other method. Para. 11; see also para.117.

As to novelty and inventive step, please note that the X-bar switch in the D1 reference ('451 patent) contains no controller or processor capable of executing a routing algorithm. The X-bar switch does not interconnect based on the execution of an algorithm; instead it interconnects based on the static setting of its control registers, which are written to by the Parallel Array Controller (PAC) before data passes through the X-bar switch. Neither the X-bar switch nor the entire system disclosed in D1 cannot route data based on information in the data as recited in the amended claims.

Moreover, the management complex may load different software into the switch controller

Cont/d.....

periodically, changing the switch's functionality. And, the software executed by the switch controller may perform several other functions in addition to routing (e.g., paras. 068; 088; 117), which makes the switch much more versatile than a simple X-bar switch. The X-bar switch of D1 does not provide this flexibility and functionality.

In section 3.3, the Examiner makes a blanket rejection of dependent claims 2-6 and 8-10 as obvious by combining D1 and D2. D2 does not disclose the claimed switch controller that executes a routing algorithm provided by the management system (as now recited in claims 1 and 7, claims 2 and 8 being cancelled).

I submit that the independent claims possess both novelty and inventive step.

With reference to section 4.1, reference signs have been introduced into the claims. The independent claims have been divided into the two-part form, following the analysis given above, to address section 4.2. The references to D1, D2 and D3 required by section 4.3 have been inserted at paragraphs 009a-c.

The references to documents being "incorporated by reference" have been removed from pages 27 and 39. The bibliographic data required by the closing paragraph of section 4.4 has been inserted on page 27. I found no reference to the document on page 81.

The typographical errors referred to in section 4.5 have been addressed, as will be apparent from the attached pages.

It is respectfully submitted that all of the points raised have now been met and that this application now complies with the requirements of the European Patent Convention. The Examiner is not authorised to effect any amendment to the description or claims (other than correction of obvious clerical or typographical errors) without approval. If therefore any points remain outstanding, it would be appreciated if the Examiner would contact me by telephone or, alternatively, issue a further Communication. If neither of these alternatives is acceptable and the Examiner is minded to reject the application, I respectfully request Oral Proceedings be appointed as a precaution. The applicants reserve the right to reintroduce any subject matter deleted from this application, or to file a divisional application directed to such deleted subject matter.

Yours faithfully,

R.J. BARTLE
Professional Representative
Association No. 105

Encs.
Amended set of claims in full
Track changes of the claims
Amended pages 3, 4, 5, 10, 12, 15, 16, 24, 27, 31, 37, 39 and 64 of the specific description
Manuscript pages

EXHIBIT 5

W. P. THOMPSON & Co

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• EUROPEAN TRADE MARK ATTORNEYS • REGISTERED TRADE MARK AGENTS •

Coopers Building, Church Street, Liverpool, L1 3AB
TELEPHONE: 0151 709 5961 FACSIMILE: 0151 709 0162/0151 708 8602
EMAIL: liverpool@wpt.co.uk WEBSITE: www.wpt.co.uk

14th June 2010

Electronic Transmission

EUROPEAN PATENT OFFICE
D-80298 Munich
GERMANY

Dear Sirs,

Re: European Patent Application No. 09153548.4
RING TECHNOLOGY ENTERPRISES LLC
Our Ref: RJB/CE/P420137EP

I refer to the Communication pursuant to Article 94(3) EPC dated 4th December 2009. I note that the response term has been extended to a total of six months from notification, and that notification is deemed to have taken place on 14th December 2009, whence the present response arrives in good time.

I file herewith amended versions of pages 3, 4, 5, 10, 12, 15, 16, 24, 27, 31, 37, 39 and 64 of the specific description and an amended set of claims in full.

Also attached is a second copy of the claims upon which the current amendments are highlighted.

Nonetheless let me briefly summarise the effect of the amendments, and the basis for them.

In claim 1, it is now specified that the one or more switches comprise *a configurable switch fabric (206)*. Additionally, the claim specifies that the switching is *determined by applying the data block identifier to an algorithm that selectively configures operation of the switch fabric*. Support for these amendments is to be found at least in the following paragraphs of the published specification of EP 2060976 - 0044-0045, 0068, 0087-0091, 0094-0096, 0114-0117, 0126, 0133, 0137, and also in Figures 6 and 7.

Claim 9 has been similarly amended.

Claim 16 has been deleted. Please note that this is done without the intention to abandon the subject matter of that claim, and that the applicant wishes to reserve its right to file a separate divisional in respect of the subject matter of claim 16.

Cont.d/...(2)

Reference numerals have been inserted in the claims.

In the description, a reference has been inserted to D1, the only X citation.

The paragraph on page 64 quoted in section 3.2 of the extended search report has been suitably amended to remove suggestions that the scope of the invention might be different from the scope of the claims. Mention of documents being incorporated by reference has been removed (see section 5.4 of the extended search report) and the number of the relevant granted patent has been inserted.

The clerical mistakes mentioned in section 5.5 have been attended to.

With reference to section 5.6, you are hereby authorised to cancel pages 64a-64z. This is done without prejudice to the right of the applicant to reinstate the subject matter of those pages in the present application or in a divisional.

With reference to section 2 of the extended search report, following the deletion of claim 16 there is clearly no contravention of Rule 43(2) EPC.

With reference to section 3.1, some of the objections set out therein have likewise been addressed by deletion of claim 16. I note the direction to harmonise the independent claim in different categories and have of course inserted essentially the same features into both claims 1 and 9, but I submit that those distinctions that remain between the two claims reflect properly the fact that one is directed to a system and the other to a method and that no lack of clarity arises.

The clarity objection in section 3.2 has been addressed as mentioned above.

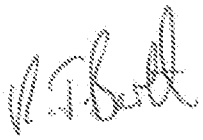
Section 4 concerns alleged lack of novelty. In this regard please note that the D1 reference does not describe or suggest one or more switches comprising a configurable switch fabric, for receiving a data request including a data block identifier and switching the data request to one or more of the memory sections determined by applying the data block identifier to an algorithm that selectively configures operation of the switch fabric, as recited in claim 1 and in claim 9. The D1 reference does not describe or suggest such a switch that includes a selectively configurable switch fabric. These features provide switches that are configurable and growable giving significant advantages over the prior art. As stated in paragraph [0142], as the storage hub's capacity is increased, the performance seen by any given user preferably remains uniform as the system grows, and expected response times for users with applications generating random data requests preferably remains uniform as the system expands. Consequently, in my submission, claims 1 and 9 are novel and provide inventive step over D1.

Cont.d/...(3)

Please note that I have not divided the claims into the two-part form and request that in this particular instance the one-part form should be allowed to remain. The reader is able to establish the relevance of D1 from the acknowledgment of it in the opening part of the description. In my submission the rearrangement needed to place the claim in two-part form would not render it more clear for the reader.

It is respectfully submitted that all of the objections raised have now been met and that this application complies with the requirements of the EPC and of the Rules made thereunder. However, the Examining Division is not hereby authorised to effect any amendment to the description or the claims, other than correction of obvious clerical or typographical errors, without approval. Therefore if any points remain outstanding, it would be appreciated if the Primary Examiner would contact me by telephone or, alternatively, issue a further Communication. As a precaution, I request that in the event that neither of these alternatives is acceptable and the Examining Division is minded to reject this application, Oral Proceedings should instead be appointed. The applicant reserves the right to reintroduce any subject matter deleted from this application or to file a divisional application directed to such deleted subject matter.

Yours faithfully,



R.J. BARTLE
Professional Representative
Association No. 105

Enc: as above

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EXHIBIT 6

PATENT
Customer No. 22,852
Attorney Docket No. 08812.0005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
M. James Bullen et al.	)	Group Art Unit: 2189
	)	
Application No.: 10/284,268	)	Examiner: Behzad Peikari
	)	
Filed: October 31, 2002	)	
	)	
For: METHODS AND SYSTEMS FOR AN IDENTIFIER-BASED MEMORY SECTION (as amended)	)	Confirmation No.: 8808

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY TO REQUEST FOR INFORMATION

In reply to the Office Action mailed April 11, 2007, the period for response to which extends through October 11, 2007, with a five-month extension of time filed concurrently herewith, Applicants submit the requested information in the Remarks section of this paper.

REMARKS

In this Reply, Applicants supply the information requested by the Examiner under 37 CFR § 1.105.

Requirement (A) - Switches

In the Request for Information ("OA"), the Examiner asked "what applicant considers a prior art switch and the state of the art for switching technology at the time of the invention." (OA at 2).

In response, Applicants are confused by what the Examiner is seeking. For example, Applicants state that at the time of the application filing date, at least certain types of fast cross-bar switches, time-division multiplexed switches, space-division multiplexed switches, fibre channel switches, ATM switches, Ethernet switches, switched-FDDI switches, IP switches, and OC-x switches were within the state of the art for switching technology. Applicants state that they have submitted several information disclosure statements citing many prior art references that disclose prior art switching technology and the state of the art of switching technology at the time the application was filed. Applicants note, however, that no prior art search has been conducted to respond to this Request.

Requirement (B) - Improvements

In the Request for Information, the Examiner asked "for identification of what is being improved." (OA at 2).

In response, Applicants state that for this Application No. 10/284,268, (Att. Docket No. 08049.0005), the improvements being claimed relate to the memory section of a storage system, which includes a novel combination of a memory device, memory

section controller, and memory interface device, and to methods of accessing data in the memory section, as recited in independent claims 1, 14, 20, and 30. The memory device, memory section controller, and memory interface device have novel, improved interconnections and inter-functionality, as recited in the claims. The specification provides detailed descriptions of embodiments consistent with the independent claims in, for example, Figures 5, 6, 7, and 16 and in the paragraphs describing those figures, among other places.

In the Request for Information, the Examiner argued that "the claims do not reflect the configurability [of the switch] and how it is achieved" and asked "[a]re amendments similar to the most recent amendments in copending application 10/284,278 needed?" (OA at 2).

In response, Applicants state that this application has claims to subject matter other than Application No. 10/284,278, (Att. Docket No. 08049.0004). The independent claims of this application relate to the memory section of the storage system, and the independent claims of this application do not recite a switch, as is recited in the independent claims of Application No. 10/284,278.

Applicants submit that with regard to dependent claims 8, 9, 17, 18, 19, 25, and 26 of this application, which recite "a switch," Applicants believe the features of the independent claims from which they depend render these claims patentable without the need for amendments.

Requirement (C) Claimed Subject Matter

In the Request for Information, the Examiner asked the Applicants to "[p]lease state the specific improvements of the subject matter in the claims over the prior art

disclosed in response to requirement (A) above and indicate the claimed subject specific elements in the claimed subject matter that provide those improvements." (OA at 2).

In response, Applicants state that this application is directed to the memory section. The memory section includes the devices, and their interconnections and functions recited in the independent claims. Specifically, the memory section includes a "memory device," a "memory section controller," and a "memory interface device," each having the functionality recited in independent claims 1, 14, 20, and 30.

Applicants do not understand how they can "state the specific improvements of the subject matter in the claims over the prior art disclosed in response to requirement (A) above," because the claimed memory section and the prior art switches identified in requirement (A) are different devices that perform different functions. As shown, for example, in the embodiment of Figure 6, the claimed memory section 30 connects to a switch 22 and, in this embodiment, operates in combination with the switch 22. When the memory section 30 is used in combination with the switch 22, as shown in the embodiment of Figure 6, each of the two devices adds its own functionality to the overall storage system. Moreover, as demonstrated by the independent claims, the memory section 30 need not be used with a switch 22. The memory section functions independently of the switch 22 and may be used without the switch 22. Thus, Applicants do not believe that it is feasible to identify "specific improvements" of the claimed memory section over the prior art switches because the memory section is a device that may be used in conjunction with the switch, not a device that replaces it.

The claimed memory section performs functions in addition to the functions performed by the prior art switches. For example, as shown in the embodiment of Figure 5, the claimed memory section includes a section controller 54, which may include a processor and memory that allow a storage system employing the claimed memory section 30 to be flexibly scaled to larger or smaller sizes and to use a changeable data routing configuration for accessing data in a memory device 66. The section controller 54 may also perform additional functions. For another example, as exemplified in many of the dependent claims, the section controller 54 may manage diagnostic and fault detection functions for the memory section 30, communicate with and be managed by the management complex 26, or perform fault correction functions, in addition to its data access management functions. None of these functions are contemplated by, or within the capabilities of, the prior art switches.

In the Request, the Examiner directed "[f]or any claims expressed as means or steps plus function, please provide the specific page and line numbers within the disclosure which describe the claimed structure and acts." (OA at 2-3).

In response, by ways of examples only, Applicants state that in claim 30, the "means for storing data" refers to at least, a memory device structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7 and 16 and related text, including for example paragraphs 73, 74, 77, 82, 83, 110, 111, 115, 117, 118, and 121-151. The "means for controlling" refers to at least one of a memory section controller structure, and a section controller structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7 and 16 and related text, including for example paragraphs 73, 75-78, 83, 84, 115-

120, 122, 131, 132, 140, 142, 143, 146, 153, and 154-166. The "means for receiving a data request" refers to at least one of a memory section controller structure, a section controller structure, a CCI circuit, an S-Portal structure, and a communications channel interface structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 9 and 16 and related text, including for example paragraphs 73, 78, 83, 115, 125, and 160. The "means for determining one or more addresses" refers to at least one of a memory section controller structure, a section controller structure, a resident memory structure, an internal controller memory structure, and a control processor, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7 and 16 and related text, including for example paragraphs 125, 126, 129, 160, and 164. The "means for determining an identifier" refers to at least one of a memory section controller structure and a section controller structure, and components and equivalents thereof, described in the specification in, among other places, Figures 1, 5-7, 11, and 16, and related text, including for example paragraphs 73, 75-78, 83, 84, 115-120, 122, 131, 132, 140, 142, 143, 146, 153, and 154-166. The "means for transferring a control signal" refers to at least one of a memory section controller structure, a section controller structure, a memory device control circuitry, memory interface device structure, timing circuitry, and a memory latch structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 15, and 16 and related text, including for example paragraphs 11, 78, 130, and 146. The "means for accessing data" refers to at least one of a memory interface device structure, temporary storage interface device structure, bus interface structure, and a memory device control circuitry structure, and

components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 9-11, 15, and 16, and related text, including for example paragraphs 11, 73-75, 78, 80, 89, 99, 100, 102, 105-110, 117, 118, 128-130, 143-151, and 158. The "means for receiving from the means for storing" refers to at least one of a memory interface device structure and a read shift register chain structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 9-11, 15, and 16 and related text, including for example paragraphs 11, 73-75, 78, 80, 89, 99, 100, 102, 105-110, 117, 118, 128-130, 143-151, and 158. The "means for receiving from the means for controlling" refers to at least one of a memory interface device structure, a bus interface, and a chain shift register structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 9-11, 15, and 16 and related text, including for example paragraphs 11, 73-75, 77, 78, 80, 89, 99, 100, 102, 105-110, 117, 118, 128-130, 135, 143-151, and 158. The "means for combining" refers to at least one of a memory interface device structure, a bus interface, a read selector structure, and a read shift register chain structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 9-11, 15, and 16 and related text, including for example paragraphs 109, 129, 130, 133, 148, 149, 161, and 162. And, the "means for forwarding" refers to at least one of a memory interface device structure, a bus interface, a selector structure, a section controller structure, a communications channel interface structure, a communications interface structure, a switch structure, and a switch fabric structure, and components and equivalents thereof, described in the specification in, among other places, Figures 2, 5-11, 15, and 16, and related text,

including for example paragraphs 11, 73-78, 80, 83, 84, 86-110, 115-120, 122, 128-130, 131, 132, 140, 142, 1443-151, 153, and 154-166.

Conclusion

Applicants believe that an interview with the Examiner to further explain responses to the information Request, including differences between the memory section subject matter claimed in this application and the switching subject matter claimed in Application No. 10/284,278, (Att. Docket No. 08049.0004), would help advance this case. The Examiner is invited to contact the Applicants' undersigned representative for an interview to discuss or expand upon any of Applicants' responses and to discuss additional aspects of the invention.

In view of the foregoing remarks, Applicants respectfully request reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: October 11, 2006

By: William J. Brogan

William J. Brogan
Reg. No. 43,515
Tel. 571-203-2748

EXHIBIT 7

Interview Summary	**Application No.** 10/284,278	**Applicant(s)** BULLEN ET AL.	
	Examiner B. James Peikari	**Art Unit** 2189	

All participants (applicant, applicant's representative, PTO personnel):

(1) *B. James Peikari (USPTO)*.

(2) *Steven Dodd (Inventor)*.

(3) *William J. Brogan (Applicant's Rep, #43,515)*.

(4)_____.

Date of Interview: *07 December 2006*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1-27*.

Identification of prior art discussed: *Ulug, U.S. 4,510,599*.

Agreement with respect to the claims f)☐ was reached. g)☐ was not reached. h)☒ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *See Continuation Sheet*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

_____
Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: The parties discussed the features of the invention. The examiner asked questions about particular claim language, including "data block identifier" and "switch". Applicant and his representative provided detailed and insightful answers to these questions, describing how the switch is configurable and "growable" and discussing features of the management device for the switch, with particular emphasis on claim 27. The examiner suggested that certain features of the independent claims may need to be more clearly defined and indicated that further consideration and search may be necessary. .

EXHIBIT 8

PATENT
Customer No. 22,852
Attorney Docket No. 08812.0004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Melvin James BULLEN et al.	Group Art Unit: 2189
Application No.: 10/284,278	Examiner: Behzad Peikari
Filed: October 31, 2002	
For: METHODS AND SYSTEMS FOR A STORAGE SYSTEM WITH A PROGRAM-CONTROLLED SWITCH FOR ROUTING DATA (as amended)	Confirmation No.: 8809

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUPPLEMENTAL AMENDMENT

In response to the Examiner's request during the telephonic interview of December 7, 2006, and in response to the Office communication mailed December 28, 2006, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims in this paper.

Remarks/Arguments follow the amendment section of this paper.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A storage system comprising:

one or more memory sections, including

one or more memory devices including storage locations that store data, and

a memory section controller that provides addresses to the memory devices, the addresses identifying storage locations for a memory device,

wherein the memory devices use the provided addresses to perform a function selected from the set of reading out and writing data to/from the memory devices; and

one or more switches, comprising a configurable switch fabric, that receive a data request including a data block identifier and switch the data request ~~based on the data block identifier~~ to one or more of the memory sections determined by applying the data block identifier to an algorithm that selectively configures operation of the switch fabric, the data block identifier identifying a set of storage locations;

wherein the memory sections to which the data request was switched forward the received data block identifier to its memory section controller which maps the data block identifier to a set of addresses for the storage locations identified by the data block identifier, and provides the set of addresses to one or more of the memory section's memory devices.

2. (Currently Amended) The storage system of claim 1, further comprising

a management system that provides [[an]] the algorithm to at least one of the one or more switches, wherein the switch executes the algorithm in switching the data request based on the data block identifier.

3. (Previously Presented) The storage system of claim 2, further comprising:

a management system that performs fault management in response to a fault being detected.

4. (Previously Presented) The storage system of claim 3, wherein the management system detects a fault with regard to a memory section in response to not receiving a message from the memory section.

5. (Previously Presented) The storage system of claim 3, wherein one or more of the memory sections include a fault detection component that detects a fault in the memory section.

6. (Previously Presented) The storage system of claim 3, wherein the management system includes:

one or more control processors for performing fault management; and

one or more administration processors that collect statistical data from the one or more switches and the one or more memory sections.

7. (Previously Presented) The storage system of claim 1, further comprising:

a management system that instructs the storage system to store a backup of data stored by one or more of the memory sections into a non-volatile storage device connected to at least one of the switches, receives a fault message from a memory section, and instructs the storage system to load the back-up of the memory section's data from the non-volatile storage device into a functioning memory section.

8. (Previously Presented) The storage system of claim 1, further comprising

an interface that connects to an external management system such that configuration management is performed through the external management system.

9. (Previously Presented) The storage system of claim 1, further comprising:

one or more memory interface devices that receives from at least one of the memory devices data stored in the storage locations identified by the addresses, combines the data with an identifier for use in forwarding the requested data, and forwards the data to one or more of the switches;

wherein the switches to which the data was forwarded switch the data using the identifier and forward the data to a destination device.

10. (Original) The storage system of claim 9, wherein the identifier for use in forwarding the requested data is an address for a device to which the data are to be forwarded.

11. (Original) The storage system of claim 9, wherein the identifier for use in forwarding the requested data is an identifier for identifying the data that are to be forwarded.

12. (Previously Presented) The storage system of claim 9, wherein the memory devices include outputs, and wherein at least one of the memory interface devices includes:

at least one set of shift registers interconnected in series, wherein at least one of the shift registers receives a clock signal having a shift frequency, and wherein the shift register shifts data loaded into the shift register to a next one of the shift registers in the set according to the shift frequency; and

wherein data from one or more of the output of a memory device is loaded into a corresponding shift register in the sets of shift registers and the loaded data is shifted from the shift register to a next one of the shift registers in the set according to the shift frequency, such that the shift register maintains its shift frequency during any loading of the data.

13. (Previously Presented) The storage system of claim 9, wherein the memory devices include outputs, and wherein at least one of the memory interface devices includes:

at least one set of shift registers interconnected in series, wherein at least one of the shift registers receives a clock signal having a shift frequency, and wherein the shift

register shifts data loaded into the shift register to a next one of the shift registers in the set according to the shift frequency; and

wherein data in the set of shifted register is loaded according to the clock signal from one or more shift registers in the set into one or more of the memory devices via an input corresponding to the shift register, such that the shift register maintains its shift frequency during any loading of the data.

14. (Previously Presented) The storage system of claim 1, wherein at least one memory section further includes

a temporary storage device that stores data to be written to a memory device; and

a temporary storage interface device that stores data in and retrieves data from the temporary storage device;

wherein at least one of the switches, in response to receiving data to be stored in the memory section, forwards the data to the temporary storage interface device, and wherein the temporary storage interface stores the data in the temporary storage device if a memory device to which the data is to be written is busy, and wherein the temporary storage interface device retrieves the data from the temporary storage device when the memory device is no longer busy and forwards the data to the memory device such that the memory device stores the data.

15. (Previously Presented) The storage system of claim 1, wherein at least one memory section further includes at least one communications channel interface for

receiving data to be stored by the memory section and transferring the data to be stored to one or more of the memory devices, and wherein the communications channel interface receives data read from the memory devices and transfers the data read from the memory devices to one or more of the switches, and wherein the communications channel interface receives data requests and forwards the data requests to the memory section controller.

16. (Currently Amended) A method for use in a storage system, comprising:

storing data in storage locations in a memory device;

receiving by a switch comprising a configurable switch fabric, a data request including a data block identifier;

the switch switching the data request ~~based on the data block identifier~~ to a memory section including the memory device determined by applying the data block identifier to an algorithm that selectively configures operation of the switch, the data block identifier identifying a set of storage locations in the memory device;

forwarding the received data block identifier to a memory section controller;

the memory section controller mapping the data block identifier to a set of addresses for the storage locations identified by the data block identifier; and

the memory section controller providing the set of addresses to the memory device; and

the memory device using the provided addresses to perform a function selected from the set of reading and writing data to/from the memory device.

17. (Currently Amended) The method of claim 16, further comprising

a management system providing [[an]] the algorithm to the switch; and

the switch executing the algorithm in switching the data request based on the data block identifier.

18. (Original) The method of claim 17, further comprising:

a management system performing fault management in response to a fault being detected.

19. (Original) The method of claim 18, further comprising:

the management system detecting a fault in response to not receiving a message from the memory section controller.

20. (Original) The method of claim 18, further comprising:

the memory section controller detecting a fault.

21. (Original) The method of claim 16, further comprising:

storing a back-up of data stored by the memory device into a non-volatile storage device connected to the switch;

a management system receiving a fault message from the memory section controller; and

the management system instructing the non-volatile storage device to send the back-up of the memory device's data to a functioning memory device.

22. (Original) The method of claim 16, further comprising:

a memory interface device receiving from the memory device data stored in the storage locations identified by the addresses;

the memory interface device combining the data with an identifier for use in forwarding the requested data;

the memory interface device forwarding the data to the switch;

the switch switching the data using the identifier; and

the switch forwarding the data to a destination device.

23. (Original) The method of claim 16, further comprising:

a memory interface device in the memory section receiving, in response to the memory section receiving a data request, data from a memory device;

shifting data in one or more shift registers in a set of shift registers interconnected in series from the shift register to a next one of the shift registers in the set on the basis of a clock signal having a shift frequency, wherein the shift registers are included in the memory interface device;

loading data from the memory device into a corresponding shift register in the set; and

shifting the data loaded into one or more of the shift registers to a next one of the shift registers in the set according to the clock signal, wherein the shift register maintains its shift frequency during the loading of the data from the memory devices into the shift registers.

24. (Original) The method of claim 16, further comprising:

a memory interface device in the memory section receiving, in response to the memory section receiving a data request, data from a memory device;

shifting data in one or more shift registers in a set of shift registers interconnected in series from the shift registers to a next one of the shift registers in the set on the basis of a clock signal having a shift frequency, the shift registers included in the memory interface device;

loading data from one or more of the shift registers to a memory device; and

shifting the data loaded from the one or more shift registers to a next one of the shift registers in the set according to the shift frequency after the data is loaded into the memory device, wherein the shift register maintains its shift frequency during the loading of the data.

25. (Previously Presented) The method of claim 16, further comprising:

the memory section receiving data to be stored in the memory device;

forwarding the data to a temporary storage interface device;

the temporary storage interface device storing the data in a temporary storage device if the memory device to which the data is to be written is busy;

the temporary storage interface device retrieving the data from the temporary storage device when the memory device to which the data is to be stored is no longer busy; and

the memory device storing the data.

26. (Currently Amended) A storage system, comprising:

means for storing, including:

means for storing data in storage locations, the means for storing data in storage locations including means for reading data stored in the storage locations using an address;

means for controlling the means for storing, the means for controlling including:

means for mapping a data block identifier to a set of addresses,

means for providing the addresses to the means for storing data in storage locations, the addresses identifying storage locations;

means for switching, including

means for receiving a data request including a data block identifier;

means for switching the data request based on the data block identifier to a means for storing determined by applying the data block identifier to an algorithm that selectively configures operation of the means for switching, the data block identifier identifying a set of storage locations in the means for storing data in storage locations; and

means for forwarding the received data block identifier to the means for storing.

27. (Currently Amended) A storage hub comprising

a memory section, including

a memory device including storage locations that store data, and

a memory section controller that provides an address to the memory device, the address identifying a storage location,

wherein the memory device uses the provided address to write data into the memory device; and

a switch, comprising a configurable switch fabric, that receives a data request including a data block identifier and transmits the data request to the memory section determined by applying the data block identifier to an algorithm that selectively configures operation of the switch fabric, and that receives write data associated with the data request and transmits the write data to the determined memory section;

wherein the memory section forwards the received data block identifier to the memory section controller, which determines from the data block identifier the address of a storage location and provides the address to the memory device, and the memory device stores the write data at the address.

REMARKS

As a preliminary matter, Applicants note that the claim amendments are based on the claims as they stood after entry of the amendment filed September 25, 2006, because the draft supplemental amendment submitted to the Examiner for review on December 8, 2006, was not officially filed or entered.

Applicants wish to thank the Examiner for his courtesy, help, and professionalism during the telephonic interview held December 7, 2006, with co-inventor Steven Dodd and Applicants' representative. Applicants feel that the discussion significantly increased understanding of the issues on both sides and greatly benefited prosecution of this application.

After submitting a draft supplemental amendment for review by the Examiner on December 8, 2006, and receiving the Examiner's comments in the Office communication mailed December 28, 2006, Applicants have finalized it into this Supplemental Amendment and hereby file it with the Office.

In this Supplemental Amendment, Applicants have amended claims 1, 2, 16, 17, 26, and 27 to clarify aspects of the invention, including some noted by the Examiner and discussed during the interview. Claims 1-27 are currently pending.

Applicants respectfully submit that these amendments place independent claims 1, 16, 26, and 27 in condition for allowance. Applicants further submit that claims 2-15 and 17-25 are also in condition for allowance at least by virtue of their dependence from allowable base claims.

EXHIBIT 9

REMARKS

As a preliminary matter, Applicants note that the Examiner did not include an initialed copy of the form PTO/SB/08 filed by Applicants with an IDS on March 7, 2005. Applicants request that the Examiner provide an initialed copy at the Examiner's earliest opportunity. For the Examiner's convenience, Applicants have enclosed another copy of the IDS and form PTO/SB/08 filed on March 7, 2005.

In this Reply, Applicants have amended the title and specification of the application and amended claims 1, 4-6, 15-19, 21-22, and 30 to correct typographical errors and other informalities and to expressly recite features inherent in the original words of the claims. These claims were not amended for reasons related to patentability. Claims 1-30 remain pending.

Summary

In the Office Action, the Examiner objected to the attempt to incorporate subject matter by reference because the serial numbers of the related applications were missing from the specification and objected to claims 1, 4, 5, and 6 for informalities. In addition, the Examiner provisionally rejected claims 4, 5, 8, 12-14, 17-22, 25, and 29 under the doctrine of obviousness-type double patenting in view of copending U.S. Application No. 10/284,278; rejected claims 4, 5, 21, and 22 under the doctrine of obviousness-type double patenting in view of U.S. Patent No. 6,879,526; rejected claims 4 and 30 under 35 U.S.C. § 112, second paragraph, as being indefinite; rejected claims 1-9, 11-17, 19-26, and 28-30 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4, 796,231 to Pinkham ("*Pinkham*"); and rejected claims 10, 18, and 27 under 35 U.S.C. § 103(a) as being unpatentable over *Pinkham* in view of the

Examiner's official notice. Applicants traverse these objections and rejections for the reasons given below.

Objections

In the Office Action, the Examiner objected to the attempt to incorporate the subject matter or related applications by reference because the serial numbers of the related applications were unknown at the time of filing and therefore missing from the specification. Applicants have amended the specification to insert the serial numbers. Applicants accordingly request the withdrawal of this objection. The Examiner also objected to the title as not descriptive. Applicants have provided a new descriptive title and request the withdrawal of this objection.

The Examiner also objected to claims 1 and 4-6 for informalities and typographical errors. Applicants have amended claims 1 and 4-6 to fix the informalities and errors according to the Examiner's suggestions. Applicants accordingly request the withdrawal of this objection.

Double Patenting Rejections

In the Office Action, the Examiner provisionally rejected claims 4, 5, 8, 12-14, 17-22, 25, and 29 under the doctrine of obviousness-type double patenting in view of copending U.S. Application No. 10/284,278. In accordance with M.P.E.P. §§ 804 and 1490, and without admitting or even agreeing with the Examiner's allegations of anticipation and double patenting, and while reserving the right to traverse the Examiner's allegations of anticipation or double patenting in the future, Applicants defer responding to the provisional double patenting rejection until it is the only rejection remaining in the two applications, and the examiner withdraws the provisional double-

patenting rejection as to one application and permits that application to issue as a patent, thereby converting the provisional double patenting rejection in the other applications into a double patenting rejection at the time the other application issues as a patent.

In the Office Action, the Examiner rejected claims 4, 5, 21, and 22 under the doctrine of obviousness-type double patenting in view of U.S. Patent No. 6,879,526, which recently issued from U.S. Application No. 10/284,198. In response, without admitting or even agreeing with the Examiner's allegations of anticipation and double patenting, and solely to advance prosecution while reserving the right to traverse the assertions of anticipation or double patenting, Applicants file herewith a terminal disclaimer in compliance with 37 C.F.R. 1.321(c) to overcome the rejection of claims 4, 5, 21, and 22 under the doctrine of obviousness-type double patenting. Accordingly, claims 4, 5, 21, and 22 are in condition for allowance, and Applicants request the withdrawal of the double patenting rejection of those claims.

35 U.S.C. § 112 Rejections

In the Office Action, the Examiner apparently rejected claim 4 under 35 U.S.C. § 112, second paragraph, as being indefinite because it is allegedly unclear what "a memory device" in the last clause refers to. Applicants have amended claim 4 solely to clarify to the Examiner that this refers to the antecedent one or more memory devices, and not for reasons related to patentability. Accordingly, claim 4 is in condition for allowance, and Applicants request the withdrawal of the 35 U.S.C. § 112, second paragraph, rejection.

In the Office Action, the Examiner rejected claim 30 under 35 U.S.C. § 112, second paragraph as being indefinite because it is allegedly unclear what means in the specification correspond to the means recited in claim 30. The Examiner required that the Applicants particularly, clearly, and distinctly point out what means claim 30 refers to.

In claim 30, the "means for storing data" refers to at least a memory device structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7 and 14 and related text. The "means for controlling" refers to at least a memory section controller structure, a section controller structure, a switch structure, a switch fabric structure, and a switch controller structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7 and related text. The "means for receiving a data request" refers to at least a memory section controller structure, a section controller structure, a communications channel interface structure, a switch structure, and a switch server communications interface structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-9 and 12 and related text. The "means for determining one or more addresses" refers to at least a memory section controller structure, a section controller structure, a resident memory structure, an internal controller memory structure, and a control processor, and components and equivalents thereof, described in the specification in, among other places, Figures 4-7 and related text. The "means for determining an identifier" refers to at least a memory section controller structure and a section controller structure, and components and equivalents thereof, described in the specification in, among other places, Figures 1, 5-

7, 11, 13, and related text. The "means for transferring a control signal" refers to at least a memory section controller structure, a section controller structure, a memory device control circuitry, and a memory latch structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 12, and related text. The "means for accessing data" refers to at least a memory interface device structure and a memory device control circuitry structure, and components and equivalents thereof, described in the specification in, among other places, Figures 1, 5-7, 9, 11, 13, and related text. The "means for receiving from the means for storing" refers to at least a memory interface device structure and a read shift register chain structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 9, 11, 13, and related text. The "means for receiving from the means for controlling" refers to at least a memory interface device structure and a chain shift register structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 9, 11, 13, and related text. The "means for combining" refers to at least a memory interface device structure and a read shift register chain structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 9, 11, 13, and related text. And, the "means for forwarding" refers to at least a memory interface device structure, a selector structure, a section controller structure, a communications channel interface structure, a communications interface structure, and a switch fabric structure, and components and equivalents thereof, described in the specification in, among other places, Figures 5-7, 9, 11, 13, and related text.

Applicants have particularly, clearly, and distinctly pointed out structures that claim 30 refers to. Accordingly, claim 30 is in condition for allowance, and Applicants request the withdrawal of the 35 U.S.C. § 112, second paragraph, rejection.

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4, 796,231 to *Pinkham* ("*Pinkham*"). The Examiner also incidentally alleged that U.S. Patent No. 4,510,599 to *Ulug* ("*Ulug*") and U.S. Patent No. 6,728,799 to Perner et al. ("*Perner*") also anticipate claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b), but did not rely on *Ulug* or *Perner* as a specific basis for rejection. Applicants traverse the rejection of claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b).

In order to properly anticipate claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b), *Pinkham* must explicitly disclose each and every limitation recited in the claims. *See* M.P.E.P. § 2131 (7th ed. 1998). If *Pinkham*, however, fails to expressly set forth a particular limitation, then the Examiner must show that this limitation is inherently disclosed to substantiate a claim of anticipation. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). To establish inherency, the Examiner must specifically identify extrinsic evidence that makes clear to one skilled in the art that the missing limitation "is necessarily present" in the *Pinkham* disclosure. *See id.; see also Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1269 (Fed. Cir. 1991).

Pinkham does not disclose each and every limitation recited in the claims. In general, the Office Action does not address, analyze, or compare to *Pinkham* every limitation recited in the claims. Instead, the Office Action attempts merely to match the

names of components recited in the claims with similarly named components disclosed in *Pinkham*, while improperly ignoring the functions, connections, and interactions of the components and operations expressly recited in the claims.

For example, independent claim 1 as amended recites, among other things, "a memory section controller for . . . determining an identifier for use in forwarding the requested data," and "a memory interface device for . . . receiving from the memory section controller the determined identifier for use in forwarding the requested data, combining the requested data and the determined identifier, and forwarding the requesting data to a destination device based on the determined identifier."

Pinkham teaches neither "an identifier for use in forwarding the requested data" nor a memory section controller or memory interface device having functions that use such an identifier, as recited in claim 1. *Pinkham* is silent regarding techniques for forwarding data to another device after being read out of a memory device, which is not surprising because *Pinkham* discloses a memory dedicated to a pixel display. "To display the pixel information stored in memory, data is read from memory and then organized in an interim storage medium in a serial format. As each horizontal line in the display is scanned, the pixel data is serially output and converted to video information." (Col. 1, lines 33-38). Thus, there is no need in *Pinkham* for "an identifier for use in forwarding the requested data," or functions associated with such an identifier because the data is forwarded to only one place, a video pixel display. (See, e.g., col. 1, lines 63-64; col. 2, lines 49-51; col. 4, lines 25-29; col. 11, lines 22-33; col. 23, lines 24-27).

In the Office Action at page 7, the Examiner cites to *Pinkham*'s address buffer 18, row address latch 20, column address latch 22, column decoder 30, tap latch

decode circuit 52, clock and control generator 69, and arbiter 68 as somehow teaching "a memory section controller" for, among other things, "determining an identifier for use in forwarding the requested data," as recited in claim 1. Applicants submit that the Examiner is mistaken in his reading of *Pinkham*. *Pinkham*'s address buffer 18, row address latch 20, column address latch 22, column decoder 30, and tap latch decode circuit 52 merely decode a memory address A0-A7 used to read or write to the pixel memory arrays 10, 12, 14, and 16 on a row and column basis. As *Pinkham* explains:

> An address A0-A7 is received in an address buffer 18, the output of which is input to a row address latch 20 and a column address latch 22. The row address latch 20 is controlled by the row address strobe signal RAS and the column address latch 22 is controlled by the column address strobe CAS. The row address latch 20 is output to a row address bus 24 and the output of the column address latch 22 is output to a column address bus 26. Each of the memory arrays 10-16 has associated therewith a row decoder 28 for receiving the latched row address from a row address bus 24 and a column decoder 30 for receiving the latch column address from the column address bus 26.
>
> (Col. 4, lines 50-63).
>
> Each of the shift registers 34-40 [which hold the data output by the memory arrays 10-16] has associated therewith tap latches 42, 44, 46 and 48, respectively. The tap latches 42-48 are operable to select the shift bit of the associated shift registers 34-40, respectively for output therefrom. The tap latches 42-48 are interfaced with a tap latch bus 50 which is connected to the output of a tap latch decode circuit 52. The tap latch decode circuit 52 receives the latched column address from the address bus 26 for decoding thereof. In the preferred embodiment, the tap latch decode circuit 52 and the column decoder 30 are shared functions such that only one decode circuit is required.
>
> (Col. 5, lines 11-22).

Thus, the address buffer 18, row address latch 20, column address latch 22, column decoder 30, tap latch decode circuit 52, clock and control generator 69, and arbiter 68 do not determine an identifier for use in forwarding the requested data. They

merely decode a memory address to either write data into or read data out of the memory arrays 10-14. They perform no functions related to an identifier for forwarding the data read out of the memory arrays.

Also in the Office Action at page 7, the Examiner cites to *Pinkham*'s I/O buffer 66, and shift registers 34, 36, 38, and 40 as somehow teaching "a memory interface device for . . . receiving from the memory section controller the determined identifier for use in forwarding the requested data, combining the requested data and the determined identifier, and forwarding the requesting data to a destination device based on the determined identifier" as recited in claim 1. Applicants submit that the Examiner is mistaken. *Pinkham*'s I/O buffer 66 is used to implement a write mask feature wherein the signals W0 -W3 determine which of the memory arrays 10-16 are to have their associated I/O ports enabled. (Col. 7, lines 20-53). *Pinkham*'s shift registers 34, 36, 38, and 40 are used to serialize the data output from memory arrays 10-16 for eventual display by video pixel display. (Abstract; Col. 5, lines 11-41).

Thus, the I/O buffer 66, and shift registers 34, 36, 38, and 40 do not receive from the memory section controller the determined identifier for use in forwarding the requested data, combine the requested data and the determined identifier, and forward the requesting data to a destination device based on the determined identifier. They merely implement a write mask and serialize the output of the memory arrays 10-14. They perform no functions related to an identifier for forwarding the data read out of the memory arrays.

Ulug and *Perner* similarly lack any teachings or suggestions related to an identifier for use in forwarding the requested data.

For at least the foregoing reasons, *Pinkham* fails to disclose each and every element recited in independent claim 1, and therefore claim 1 is allowable over *Pinkham*. Similarly, independent claims 14, 20, and 30, which recite features similar to those recited in claim 1, are also allowable for at least the same reasons. In addition, dependent claims 2-13, 15-19, and 21-29 are allowable at least by reason of their dependence from allowable independent claims 1, 14, and 20 respectively. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Regarding claims 2, 3, 9, 15, 16, and 26, as explained above *Pinkham* does not teach or suggest anything related to an identifier for use in forwarding the requested data as recited in these claims. *Ulug* and *Perner* similarly lack any teachings or suggestions related to an identifier for use in forwarding the requested data as recited in these claims.

For at least this additional reason, *Pinkham* fails to disclose each and every element recited in claims 2, 3, 9, 15, 16, and 26, and therefore these claims are allowable over *Pinkham*. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Regarding claims 4-6 and 21-23, *Pinkham* does not teach or suggest each and every element recited in these claims. For example, claim 4 as amended recites, among other things, "such that the shift register maintains its shift frequency during any loading of the data." *Pinkham* does not teach or suggest anything related to the concept that the shift register maintains its shift frequency during any loading of the

data. *Pinkham* merely discloses conventional shift registers that cannot shift and load data at the same time. *Ulug* and *Perner* do not supply this missing element either.

For at least this additional reason, *Pinkham* fails to disclose each and every element recited in claim 4, and therefore claim 4 is allowable over *Pinkham*. Similarly, claims 5, 6, and 21-23, which recite features similar to those recited in claim 4, are also allowable for at least the same additional reason. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Regarding claims 8, 9, 17-19, 25, and 26, *Pinkham* does not teach or suggest switches with the features and functions recited in these claims. Although *Pinkham* discloses single pole double throw switches, the switches in *Pinkham* are not at all like those recited in claims 8, 9, 17-19, 25, and 26. The switch is *Pinkham* is an "A/B switch" (56, 58, 60, 62) that merely directs the output of a tap latch (42, 44, 46, 48) to either: A) the input of the shift register being tapped as a circulating shift register, or B) the input of another cascaded shift register. (Col. 5, line 42 - col. 6, line 54; Fig. 1). *Pinkham*'s switches do not perform any of the functions of the switches recited in claims 8, 9, 17-19, 25, and 26. *Pinkham*'s switches do not receive a control signal from the memory section controller that indicates which of the one or more communications paths to use to send the requested data, as recited in claims 8 and 25. They do not receive anything. *Pinkham*'s switches do not use an identifier to forward the requested data to the destination device, as recited in claims 9 and 26. They have no intelligence, such as a processor or internal memory, able to recognize an identifier. *Pinkham*'s switches do not use algorithms, employ a management system, or direct data requests, as recited in claims 17-19. The switches in *Pinkham* are used to configure shift register

output connections; they are merely single pole double throw switches that switch the shift registers between circulating and cascade mode based on whether they are thrown to one circuit path or the other. Single pole double throw switches simply do not have the capability to operate based on an identifier or algorithm, or to direct a data request. Furthermore, nothing else disclosed in *Pinkham* (or *Ulug* or *Perner*) performs these functions.

For at least this additional reason, *Pinkham* fails to disclose each and every element recited in claims 8, 9, 17-19, 25, and 26 and therefore these claims are allowable over *Pinkham*. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 10, 18, and 27 under 35 U.S.C. § 103(a) as being unpatentable over *Pinkham* in view of the Examiner's official notice of memory fault detection and protection techniques allegedly known in the art. Applicants traverse.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, the Examiner must demonstrate that (1) *Pinkham* and the officially noticed techniques disclose or suggest each and every limitation recited in the claims; (2) there is a reasonable probability of success of any modification of the teachings of *Pinkham*, and (3) there exists some suggestion or motivation, either in the teachings of *Pinkham* itself or in the knowledge generally available to one of ordinary skill in the art, to make such a modification in a manner resulting in the claimed invention. *See* M.P.E.P. § 2143 (7th

ed. 1998). Furthermore, each of these requirements must be found in the prior art – not based on Applicants' own disclosure. *See id.*

For the reasons detailed above, *Pinkham* fails to teach or suggest several elements recited in independent claims 1, 14, and 20, from which claims 10, 18, and 27 depend. Even assuming, *arguendo*, that the Examiner's official notice of memory fault detection and protection techniques allegedly known in the art is accurate, the official notice fails to teach or suggest the elements recited in claims 1, 14, and 20 that are missing from *Pinkham*. Accordingly, because *Pinkham* combined with the Examiner's official notice fails to disclose each and every element recited in the base claims, dependent claims 10, 18, and 27 are allowable at least by virtue of their dependence from allowable claims 1, 14, and 20.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 7, 2005

By: William J. Brogan
William J. Brogan
Reg. No. 43,515

Enclosure: Copy of the IDS and form PTO/SB/08 filed on March 7, 2005.

EXHIBIT 10

REMARKS

Applicants thank the Examiner for considering the IDS filed by Applicants on March 7, 2005.

In this Reply filed with a Request for Continued Examination, Applicants have amended the specification to correct minor typographical errors, amended claims 1, 4, 6, 14, 20, 23, and 30 to correct typographical errors and other informalities and to expressly recite features inherent in the original words of the claims, and added new claims 31-37. No new matter has been introduced by these claims. Claims 1-37 are pending.

Summary

In the Office Action, the Examiner provisionally rejected claims 4, 5, 8, 12-14, 17-22, 25, and 29 under the doctrine of obviousness-type double patenting in view of the claims of copending U.S. Application No. 10/284,278; rejected claims 4, 5, 21, and 22 under the doctrine of obviousness-type double patenting in view of U.S. Patent No. 6,879,526; rejected claim 4 under 35 U.S.C. § 112, second paragraph, as being indefinite; rejected claims 1-9, 11-17, 19-26, and 28-30 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4, 796,231 to *Pinkham* ("*Pinkham*"); and rejected claims 10, 18, and 27 under 35 U.S.C. § 103(a) as being unpatentable over *Pinkham* in view of the Examiner's official notice. Applicants traverse these rejections for the reasons given below.

Double Patenting Rejections

In the Office Action, the Examiner provisionally rejected claims 4, 5, 8, 12-14, 17-22, 25, and 29 under the doctrine of obviousness-type double patenting in view of

claims 1-2, 7, and 12-16 of copending U.S. Application No. 10/284,278. In accordance with M.P.E.P. §§ 804 and 1490, and without admitting or agreeing with the Examiner's allegations of anticipation and double patenting, and while reserving the right to traverse the Examiner's allegations of anticipation or double patenting in the future, Applicants defer responding to the provisional double patenting rejection until it is the only rejection remaining in the two applications, and the Examiner withdraws the provisional double-patenting rejection as to one application and permits that application to issue as a patent, thereby converting the provisional double patenting rejection in the other applications into an actual double patenting rejection at the time the other application issues as a patent.

35 U.S.C. § 112 Rejections

In the Office Action, the Examiner rejected claim 4 under 35 U.S.C. § 112, second paragraph, as being indefinite because it is allegedly unclear what "a memory device" in the last clause refers to. Applicants have amended claim 4 to recite "a memory device of the one or more memory devices" to clarify that this refers to one of the memory devices of the antecedent one or more memory devices. Accordingly, claim 4 is in condition for allowance, and Applicants request the withdrawal of the 35 U.S.C. § 112, second paragraph, rejection.

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1-9, 11-17, 19-26, and 28-30 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,796,231 to Pinkham ("*Pinkham*"). The Examiner also alleged in passing that U.S. Patent No. 4,510,599 to *Ulug* ("*Ulug*") and U.S. Patent No. 6,728,799 to Perner et al. ("*Perner*") also anticipate

these claims. The Examiner did not, however, rely on Ulug or Perner as a basis for any rejection. Accordingly, Applicants need not respond to the allegations regarding Ulug and Perner, which are unfounded in any case. Regarding the *Pinkham* reference, Applicants traverse the rejection of claims 1-9, 11-17, 19-26, and 28-30 under 35 U.S.C. § 102(b).

Claims 1-9, 11-17, 19-26, and 28-30

In order to properly anticipate claims 1-9, 11-17, 19-26, and 28-30 under 35 U.S.C. § 102(b), the Examiner must demonstrate that *Pinkham* explicitly discloses each and every limitation recited in the claims. *See* M.P.E.P. § 2131 (8th ed., May 2004 rev.). If *Pinkham*, however, fails to expressly set forth a particular limitation, then the Examiner must show that this limitation is inherently disclosed to substantiate a claim of anticipation. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). To establish inherency, the Examiner must specifically identify extrinsic evidence that makes clear to one skilled in the art that the missing limitation "is necessarily present" in the *Pinkham* disclosure. *See id.; see also Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1269 (Fed. Cir. 1991).

Pinkham does not disclose each and every limitation recited in the claims, which include the functions, operations, connections, and interactions of the combinations of devices expressly recited in the claims.

For example, independent claim 1 as amended recites, among other things, "a memory section controller for receiving a request for data stored by the memory device . . . [and] determining a destination identifier for use in forwarding the requested data to a specific destination device," and "a memory interface device for . . . receiving from the

memory section controller the determined identifier for use in forwarding the requested data, combining the requested data and the determined identifier, and forwarding the combined requested data and identifier to the specific destination device."

For the reasons given in the last response (hereby incorporated herein by reference), Applicants maintain that *Pinkham* teaches neither "a destination identifier for use in forwarding the requested data to a specific destination device" nor a memory section controller nor memory interface device having functions that use such an identifier, as recited in claim 1.

In maintaining the section 102 rejection of claim 1, the Examiner argues that "[t]he claimed 'identifier' is merely 'for use in forwarding,'" and that *Pinkham* teaches a destination identifier for use in forwarding the requested data because "[a]n address is used to 'forward' or send, information to a memory, and shown by *Pinkham*." (Office Action at 9). The Examiner further argues that "[a]ddress decoders [as disclosed in *Pinkham*] do, indeed, 'determine an identifier for use in forwarding the requested data.'" (*Id.*) Assuming, *arguendo*, that this is accurate for writing data into a memory device as the Examiner states, it does not anticipate claim 1 because claim 1 does not recite a destination identifier (and associated devices) for writing data into a memory device. Instead, the combination of devices recited in claim 1 "receiv[e] a request for data stored by the memory device," "determin[e] a destination n identifier for use in forwarding the requested data to a specific destination device," "receiv[e] from the memory device the requested data," and "forward[] the . . . requested data . . . to the specific destination device." To clarify the function of the claimed devices with respect to the identifier that was inherent in the words of the original claim, Applicants have

amended claim 1 to recite "a memory section controller for . . . determining a destination identifier for use in forwarding the requested data to a specific destination device."

Contrary to the Examiner's contentions, *Pinkham*'s address decoder does not forward data from a memory device to a specific destination device identified by the decoded address. (Col. 2, lines 55-59; col. 4, lines 50-63; col. 6, lines 59-65). The address in the memory where the data is stored does not determine the specific destination device that the data will be forwarded to. The address decoder uses the address to locate data in the memory, not to forward data from the memory to another device. (*Id.*) As explained in the previous response, *Pinkham*'s memory system is dedicated to supplying data to a connected pixel display, thus there is no disclosure of, or need for, an identifier for use in forwarding the requested data from the memory to some device identified by the identifier other than the pixel display. (Col. 1, lines 33-38, 63-64; col. 2, lines 49-51; col. 4, lines 25-29; col. 11, lines 22-33; col. 23, lines 24-27).

Also for the reasons given in the last response, Applicants maintain that *Pinkham* does not teach "a memory interface device for . . . receiving from the memory section controller the determined identifier for use in forwarding the requested data, combining the requested data and the determined identifier, and forwarding the combined requested data and identifier to the specific destination device," as recited in amended claim 1.

In maintaining the section 102 rejection of claim 1, the Examiner contends that "the claim does not specify what type of 'combine' is performed. Accordingly, serializing data and port information could be, and is, interpreted as combining." (Office Action at 10). The Examiner does not cite to any portion of *Pinkham* as teaching "serializing data

and port information," and indeed such is not taught by *Pinkham*. Furthermore, the Examiner has adopted an unreasonably broad interpretation of "identifier" and "combine" that is at odds with the rest of the claim and inconsistent with the specification. (See, e.g., application at paras. 163, 164).

In both office actions, the Examiner cited to *Pinkham*'s I/O buffer 66, and shift registers 34, 36, 38, and 40 as disclosing the claimed memory interface device. Applicants continue to disagree. To clarify and expressly recite the inherent meaning of the original claim words regarding the function of the claimed memory interface device with respect to the identifier and combining operation, Applicants have amended claim 1 to recite "combining the requested data and the determined identifier, and forwarding the combined requested data and identifier to the specific destination device." *Pinkham* does not teach these features.

The Examiner's assertion that *Pinkham* serializes port information and memory data is inaccurate. As explained in the previous reply, the devices in *Pinkham* that the Examiner relies upon (I/O buffer 66, and shift registers 34, 36, 38, and 40) do not perform this function. Specifically, *Pinkham*'s I/O buffer 66 is used to implement a write mask to determine which of the memory arrays 10-16 can be written to. (Col. 7, lines 20-53). The write mask and I/O buffer 66 have nothing to do with data that is read out of a memory array 10-16 into a shift register 34-40. (Col. 5, lines 11-41). The shift registers 34-40 do not serialize any information about the I/O ports of the memory arrays 10-16, much less combine it with data read out of memory arrays 10-16 as the Examiner asserts. Moreover, the Office Action contends that it is the address A0-A7 that equates to the "identifier" of claim 1, not port information (Office Action at 5), but

shift registers 34-40 do not serialize the address A0-A7 in combination with the date read out of memory arrays 10-16 as the Examiner contends. In short, *Pinkham* does not disclose any device that combines the data read out of memory arrays 10-16 with a destination identifier to result in the "combined requested data and identifier" as recited in claim 1. Accordingly, *Pinkham* does not disclose "a memory interface device for receiving from the memory device the requested data stored by the memory devices, receiving from the memory section controller the determined identifier for use in forwarding the requested data, combining the requested data and the determined identifier, and forwarding the combined requested data and identifier to the specific destination device," as recited in claim 1.

For at least the foregoing reasons, *Pinkham* fails to disclose each and every element recited in independent claim 1, and therefore claim 1 is allowable over *Pinkham*. Similarly, independent claims 14, 20, and 30 are likewise not anticipated by *Pinkham* for similar reasons. In addition, dependent claims 2-13, 15-19, and 21-29 are allowable at least by reason of their dependence from allowable independent claims 1, 14, and 20 respectively. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Claims 4-6 and 21-23

As explained in the last response, dependent claims 4-6 and 21-23 are also allowable for at least one additional reason. Applicants maintain that *Pinkham* does not teach or suggest, among other things, "that the shift register maintains its shift frequency during any loading of the data," as recited in claims 4-6 and 21-23 because

Pinkham discloses conventional shift registers 34-40 that cannot load data to and from the memory arrays 10-16 while continuing to shift according to their shift frequency.

In maintaining the section 102 rejection of claims 4-6 and 21-23, the Examiner contends that:

> The shift frequency is the clock frequency that goes into the shift register. The frequency of that clock does not change, whether or not data is loaded or shifted or both. The claim does not require that data is actually shifted at the same time it is loaded.

Applicants submit that the Examiner is misinterpreting the claim language. Although the Examiner has interpreted "shift frequency" in the claims as referring to the frequency of the clock whose signals control the shift register, in claims 4-6 and 21-23 "shift frequency" refers to the frequency at which the shift register itself shifts. For example, claim 4 expressly recites "that the shift register maintains its shift frequency during any loading of the data." (Emphasis added).

For at least these additional reasons, *Pinkham* fails to disclose each and every element recited in claims 4-6 and 21-23, and therefore these claims are allowable over *Pinkham*. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Claims 8, 9, 17-19, 25, and 26

As explained in the last response, dependent claims 8, 9, 17-19, 25, and 26 are also allowable for at least one additional reason. Applicants maintain that *Pinkham* does not teach or suggest switches with the features and functions recited in these claims.

In maintaining the section 102 rejection of claims 8, 9, 17-19, 25, and 26, the Examiner contends that *Pinkham* discloses the claimed switches, control signals, and

memory section controller because *Pinkham*'s switches "must, inherently, receive a control signal of some sort – how else would they know whether or not to switch?" and because "the management system is inherently in place in *Pinkham* as different methods of operation (serial and cascaded) are used. Something has to tell the system which one to use – that would be the 'management system.'" (Office Action at 11).

Pinkham's disclosure answers the Examiner's questions and makes clear that *Pinkham* does not teach an inherent management system and control signals for its "switches." There are no inherent management systems, no inherent control signals for switching, and no inherent controller for changing from serial to cascaded mode because *Pinkham*'s "switches" are not switches—they are merely a shorthand way to illustrate two different design options that are chosen before implementation and hardwired into the circuit:

> Each of the switches 56-62 is a metal mask programmable option which is selected during fabrication of the semiconductor memory. Although illustrated as switches, they are in actuality a series of lines which are connected or disconnected on the mask prior to fabrication of the device.
>
> (Col. 5, lines 58-64; see also col. 10, lines 57-60, col. 17, lines 11-14).

Thus, *Pinkham's* "switches" do not and cannot switch and consequently do not inherently receive a control signal from an inherent management system as the Examiner contends.

Moreover, as explained in the last response, even if there were a management system that sends control signals to the switches disclosed by *Pinkham* (which there is not), the simple single pole double throw switches illustrated in *Pinkham* do not anticipate the claimed management system and intelligent switches that use the destination identifier to forward data (claims 9, 26) and use an algorithm to connect

memory sections to communication channels (claim 17), among other things. Such functionality is not inherent in a single pole double throw switch, and Pinkham fails to disclose any other devices with such functionality.

For at least these additional reasons, *Pinkham* fails to disclose each and every element recited in claims 8, 9, 17-19, 25, and 26 and therefore these claims are allowable over *Pinkham*. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

35 U.S.C. § 103 rejections of claims 10, 18, and 27

For the reasons given in the previous response, the Office Actions fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 at least because *Pinkham* and the officially noticed techniques do not disclose or suggest each and every limitation recited in the claims. As explained above, *Pinkham* fails to teach or suggest several elements recited in independent claims 1, 14, and 20, from which claims 10, 18, and 27 depend. Accordingly, because *Pinkham* combined with the Examiner's official notice of allegedly known subject matter fails to disclose each and every element recited in the base claims, dependent claims 10, 18, and 27 are allowable at least by virtue of their dependence from allowable claims 1, 14, and 20.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 21, 2006

By: William J. Brogan
William J. Brogan
Reg. No. 43,515

EXHIBIT 11

REMARKS

In this Reply , Applicants have amended claims 1-10, 12-18, 20, 23, 26, 30-32, and 34-36 to more clearly claim the subject matter of the invention and to expressly recite features inherent in the original words of the claims, and cancelled claim 37 without prejudice or disclaimer. Claims 1-36 are pending.

As a preliminary matter, Applicants strongly believe an interview with the Examiner would greatly aid the Examiner's understanding of the invention and significantly benefit prosecution of this application. Applicants hereby request an interview and invite the Examiner to contact Applicants' undersigned representative at 571-203-2748 to schedule a convenient time and date. Applicants note that they previously requested an interview with Examiner Chase, but he declined because this application was in the process of being reassigned to a new Examiner.

Summary

In the Office Action, the Examiner provisionally rejected claims 4, 5, 8, 12-14, 17-22, 25, and 29 under the doctrine of obviousness-type double patenting in view of certain claims of copending U.S. Application No. 10/284,278; objected to claim 37 under 37 C.F.R. § 1.75(c); rejected claims 4-6 and 21-23 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement; rejected claims 1-3, 7,9, 14-16, 20, 26, and 30 under 35 U.S.C. § 112, second paragraph, as being indefinite; rejected claims 1-3, 7-9, 12-17, 20, 24-26, and 29-31, and 33-37 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,510,599 to Ulug ("*Ulug*"); rejected claims 4-6, and 21-23 under 35 U.S.C. § 102(b) as being anticipated by *Ulug* with U.S. Patent No. 4, 796,231 with Pinkham ("*Pinkham*") offered as evidence of the inherent characteristics of shift registers; and rejected claims 10, 11, 18, 19, 27, 28, and

32 under 35 U.S.C. § 103(a) as being unpatentable over *Ulug* in view of the Examiner's official notice.[1] Applicants traverse these rejections for the reasons given below.

Double Patenting Rejections

In the Office Action, the Examiner provisionally rejected claims 4, 5, 8, 12-14, 17-22, 25, and 29 under the doctrine of obviousness-type double patenting in view of claims 1-2, 7, and 12-16 of copending U.S. Application No. 10/284,278. In accordance with M.P.E.P. §§ 804 and 1490, and without admitting or agreeing with the Examiner's allegations of anticipation and double patenting, and while reserving the right to traverse the Examiner's allegations of anticipation or double patenting in the future, Applicants defer responding to the provisional double patenting rejection until it is the only rejection remaining in the two applications. Applicants will respond to this rejection when the Examiner withdraws the provisional double-patenting rejection as to one application and permits that application to issue as a patent, thereby converting the provisional double patenting rejection in the other applications into an actual double patenting rejection at the time the other application issues as a patent.

Objection to Claim 37

Applicants have cancelled claim 37, making the Examiner's objection of this claim moot.

[1] To the extent the Examiner characterizes or makes assertions regarding the claims and the prior art, including the knowledge in the art at the time this application was filed, Applicants decline to automatically subscribe to any such characterizations or assertions.

35 U.S.C. § 112, First Paragraph Rejections and 35 U.S.C. § 102(b) Rejections of Claims 4-6 and 21-23

The Office Action rejected claims 4-6 and 21-23 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement and under 35 U.S.C. § 102(b) as being anticipated by *Ulug*. Applicants traverse.

In the Office Action, the Examiner states that the claim limitation "such that the shift register maintains its shift frequency during any loading of the data" is not adequately described in the specification in compliance with section 112 based on the Examiner's understanding of Applicants' arguments regarding the shift register and the relevant disclosure in the specification. Applicants submit that the Examiner has not fully understood the Applicants' arguments, and that the claimed shift register and related clocking circuitry is described in the specification in full compliance with section 112 because the specification incorporates by reference (e.g., in paras. 119, 129) the specification of U.S. Patent Application No. 10/284,198 entitled "Methods and Apparatus for Improved Memory Access" (now issued as U.S. Patent No. 6,879,526).

Regarding the first point, Applicants are not arguing "that the shift register does not shift according to the clock signal" as the Examiner states. Applicants are pointing out the fact that a conventional shift register does not maintain its shift frequency while loading data, unlike the claimed shift register. Consider the specific example where a system clock produces four clock pulses, C1, C2, C3, and C4, at the system clock's frequency. For a conventional shift register, if the shift register is not loading data in parallel to/from some device, such as a memory, during the four clock pulses, then it will shift four times at the system clock's frequency (e.g., at an edge of C1, an edge of C2,

an edge of C3, and an edge of C4) . In this situation, the conventional shift register maintains its shift frequency while it is not loading data.

If, on the other hand, the conventional shift register is loading data in parallel either into or out of a device, such as a memory, during the four clock pulses C1 - C4, the conventional shift register will not shift during one or more of the clock pulses because it takes longer than one clock pulse to perform the parallel loading of data into or out of the device. In this situation, a conventional shift register shifts less than four times during the four pulse time period, even though four clock pulses were produced by the system clock at the system clock's frequency during that time period. Thus, because the conventional shift register does not shift on every clock pulse, it does not maintain its shift frequency during any loading of data, because the conventional shift register does not shift every time the system clock produces a pulse at the clock's frequency while it is loading data in parallel.

Applicants point out that *Ulug*, *Pinkham*, and the other references cited by the Examiner disclose such conventional shift registers that do not maintain their shift frequency during any loading of the data and consequently do not teach or suggest the shift register recited in claims 4-6 and 21-23 and disclosed in detail in incorporated-by-reference U.S. Patent Application No. 10/284,198 entitled "Methods and Apparatus for Improved Memory Access" (now issued as U.S. Patent No. 6,879,526). Applicants refer the Examiner to, and hereby incorporate by reference, the response filed February 21, 2006, for Applicants' further remarks regarding why *Pinkham* does not disclose the claimed shift registers. Because the claimed shift registers are both fully described and patentable over the prior art, Applicants request that the Examiner withdraw the

rejections of claims 4-6 and 21-23 under 35 U.S.C. § 112, first paragraph and under 35 U.S.C. § 102(b).

35 U.S.C. § 112, Second Paragraph, Rejections

In the Office Action, the Examiner argued that there is insufficient antecedent basis for "the determined identifier" and "the identifier" as recited in claims 1-3, 9, 14-16, 20, 26, and 30. The Examiner also argued that the term "may be" in claim 7 is indefinite.

Applicants have amended the form of claims 1-3, 7, 9, 14-16, 20, 26, and 30 to address the Examiner's arguments, without necessarily agreeing with the arguments. Claims 1-3, 7, 9, 14-16, 20, 26, and 30 are now in form for allowance, and Applicants request that the Examiner withdraw the 35 U.S.C. § 112, second paragraph, rejection of these claims.

35 U.S.C. § 102(b) Rejections

In the Office Action, the Examiner rejected claims 1-3, 7-9, 12-17, 20, 24-26, and 29-31, and 33-37 under 35 U.S.C. § 102(b) as being anticipated by *Ulug.* In the Office Action, the Examiner explained that as an initial step in applying *Ulug* to these claims, the Examiner interpreted the claims. In so doing, the Examiner interpreted several claim recitations as "intended use" recitations (e.g., "adapted to," "capable of," "for," "in order to"), wherein if the prior art has the capability to perform the "intended use" recitation, then the recitation does not distinguish the claim from the prior art. The Examiner also questioned whether the "whereby" and "wherein" clauses in claims 4-6, 8, 11, and 12 merely state the result of a previous claim limitation, adding nothing to the patentability or substance of a claim.

Applicants have amended the form of claims 1, 3-8, 10, 12-14, 17, 18, 23, 31, 32, and 34-36 to address the Examiner's contentions regarding claim interpretation, without necessarily agreeing with the contentions. In addition, all the wherein clauses relate back to and clarify what is required by the claim, and therefore must be given patentable weight. Claims 1, 3-8, 10, 12-14, 17, 18, 23, 31, 32, and 34-36 are now in form for allowance, and Applicants request that the Examiner withdraw the 35 U.S.C. § 102(b) rejection of these claims.

In order to properly anticipate claims 1-3, 7-9, 12-17, 20, 24-26, and 29-31, and 33-37 under 35 U.S.C. § 102(b), the Examiner must demonstrate that *Ulug* explicitly discloses each and every limitation recited in the claims. *See* M.P.E.P. § 2131 (8th ed., May 2004 rev.). If *Ulug*, however, fails to expressly set forth a particular limitation, then the Examiner must show that this limitation is inherently disclosed to substantiate a claim of anticipation. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). To establish inherency, the Examiner must specifically identify extrinsic evidence that makes clear to one skilled in the art that the missing limitation "is necessarily present" in the *Ulug* disclosure. *See id.; see also Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1269 (Fed. Cir. 1991).

Applicants traverse the section 102 rejection of claims 1-3, 7-9, 12-17, 20, 24-26, and 29-31, and 33-37 at least because *Ulug* does not disclose each and every limitation recited in these claims, which include the functions, operations, connections, and interactions of the combinations of devices expressly recited in each claim.

As a preliminary matter, the Examiner rests the section 102 rejection of these claims on the basic premise that the claims contain “intended use” recitations (e.g.,

"adapted to," "capable of," "for," "in order to"), wherein if the prior art has the capability to perform the recitation, then the recitation does not distinguish the claim from the prior art. Applying this, the Examiner apparently contends that *Ulug's* microprocessors 22 and 50 in BIU 16 (Fig. 2) anticipate all the elements reciting an "intended use" because they may be "programmed to perform any function." (Office Action at 6, 8). Although not in agreement with the Examiner's premise, Applicants have amended the form of the claims to positively recite the functions of various claimed elements. Consequently, *Ulug*'s microprocessors do not anticipate these claimed elements because *Ulug* does not disclose the functions recited in the claims.

With regard to specific claims, independent claim 1 as amended recites a memory section, comprising a combination of elements including, among other things, a memory section controller that receives a request for data stored by the one or more memory devices, determines one or more addresses for the requested data, determines a destination identifier for use in forwarding the requested data to a specific destination device, and transfers a control signal to the memory devices including the determined addresses to the memory device storing the requested data; and a memory interface device that receives from the memory device the requested data stored by the memory devices, receives from the memory section controller the determined destination identifier for use in forwarding the requested data, combines the requested data and the determined destination identifier, and forwards the combined requested data and destination identifier to the specific destination device. *Ulug* does not disclose each and every one of these features.

Ulug, instead, purports to disclose a bus interface unit (BIU) that receives information packets from a bus and may or may not queue each packet before retransmission, depending on the priority of the packet and the mode of the BIU. (See, e.g., abstract; col. 1, lines 6-15; col. 2, lines 26-53). In the *Ulug* system:

> each information packet to be transmitted is assigned a predetermined priority. Each time a BIU has an information packet to transmit, it senses both a transmit and a receive bus to determine if any other information packet is on the buses. If not, the BIU places its information packet on the transmit bus. If the BIU receives an information packet on the transmit bus from an upstream BIU while it is transmitting, it compares the priority of the information being transmitted with the priority of the information packet received on the transmit bus. If the priority of the information packet received on the transmit bus is lower than the priority of the information packet being transmitted, the transmission continues and the information packet received on the transmit bus is stored by the transmitting BIU for later retransmission. If the priority of the information packet received is equal to or higher than the priority of the information packet being transmitted, the BIU immediately aborts transmission of its own information packet and begins retransmitting the equal or higher priority packet.
>
> (Col. 2, lines 27-47).

Ulug's BIU does not disclose, and in fact is fundamentally different from, a "memory section" with a "memory device," a "memory section controller," and a "memory interface device" that function as recited in claim 1 because a BIU is not designed to, and cannot, store data and forward specific data to a destination device when it receives a request for the specific data.

Ulug cannot anticipate the claims merely because it happens to disclose a device with components having names similar to the components recited in the claims, while failing to disclose the interfunctioning, connections, and interactions of the components expressly recited in the claims. For a specific example, the Office Action relies on *Ulug*'s memory control 38 (Fig. 2) for teaching the recited "memory section controller"

and relies on column 5, lines 17-25 for teaching that the memory section controller "receives a request for data stored by the one or more memory devices." (Office Action at 8, 9). As shown in Figure 2 and disclosed in column 5, lines 17-25, data may be read or written between RAM 36 and user 15 under the control of microprocessor 50. As *Ulug* clearly explains, "[u]ser 14 is coupled to random access memory (RAM) 36 through interface circuit 51 and memory controller 38." (Col. 5, lines 10-12).

This teaching of *Ulug*, however, is irreconcilable with the Examiner's assertion that *Ulug*'s memory control 38 also "determines a destination identifier for use in forwarding the requested data to a specific destination device," which is another recited function of the memory section controller in claim 1. Because user 14 is directly coupled to RAM 36, *Ulug* does not teach that memory controller 38 "determines a destination identifier for use in forwarding the requested data to a specific destination device," and indeed there is no need for it to perform such a function. As Figure 2 and column 5, lines 10-25 show, the data read out of RAM 36 under the control of microprocessor 50 can go nowhere except to user 14. Consequently, there is no logical reason why *Ulug*'s memory controller 38 would "determine[] a destination identifier for use in forwarding the requested data to a specific destination device" as the Examiner asserts.

Moreover, the portion of *Ulug* cited by the Examiner to support this assertion does not refer to the same components and functions of *Ulug*'s BIU that the Examiner asserts disclose the other features of the memory section controller recited in claim 1. Specifically, the Examiner relies on column 1, lines 25-35 of *Ulug* as disclosing that the memory section controller "determines a destination identifier for use in forwarding the

requested data to a specific destination device." (Office Action at 9). This portion of *Ulug*, however, relates to how a BIU forms an information packet, including a destination address, that it places on the transmission bus for transmission to another BIU. This teaching is unrelated to the transfer of data between RAM 36 and user 14 under the control of microprocessor 50, because user 14 is directly coupled to RAM 36 and is not connected to the transmission bus. The Examiner's position is not supported by the teachings of *Ulug* because on the one hand the Examiner asserts that the "destination identifier for use in forwarding the requested data to a specific destination device" refers to an identifier for user 14 (which is not connected to the bus), and on the other hand asserts that the same "destination identifier" refers to an identifier for a device on the bus. (Office Action at 8).

There are other inconsistencies and misinterpretations of *Ulug* in the Examiner's rejection, such as asserting that the claimed "memory interface device" is disclosed by *Ulug*'s BIU 16 in Figure 2. Figure 2, however, discloses that BIU 16 includes memory controller 38 and RAM 36, which the Examiner asserts teach the claimed "memory section controller" and "memory device," respectively. According to this assertion, the BIU 16, which includes RAM 36, would have to somehow "receive from the memory device [RAM 36] the requested data stored by the memory device [RAM 36]" and the BIU 16, which includes memory controller 38, would have to somehow "receive[] from the memory section controller [memory controller 38] the determined destination identifier for use in forwarding the requested data." In a similarly inconsistent example, the Examiner asserts that "determining one or more addresses for the requested data" as recited in claim 1 is taught by the inherent addresses of *Ulug*'s RAM 36, and also

asserts that the exact same "determined addresses" recited in claim 7, which depends from claim 1, are taught by the packets transmitted on the transmission bus. (Office Action at 10). This is illogical because the addresses of RAM 36 are separate, different, and unrelated to the address in the header of a data packet on the transmission bus. As noted above, while a BIU may have similarly named components, it simply does not function to store data, receive a request for specific data and forward the specific data to a destination device according to a destination identifier like the memory section recited in claim 1.

For at least the foregoing reasons, *Ulug* fails to disclose each and every element recited in independent claim 1, and therefore claim 1 is allowable over *Ulug*. Similarly, independent claims 14, 20, and 30 are likewise not anticipated by *Ulug* for similar reasons. In addition, dependent claims 2-13, 15-19, and 21-29 are allowable at least by reason of their dependence from allowable independent claims 1, 14, and 20 respectively. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Several of the dependent claims are also allowable for additional independent reasons. For example, claims 9 and 26 recite, among other things, switches that use the destination identifier to forward data. Claim 17 recites, among other things, a switch and managernent system that use an algorithm to connect memory sections to communication channels. The simple switches controlled by a signal from a microprocessor indicating which of three modes the BIU is in as disclosed by *Ulug* (e.g., col. 5, lines 26-32; col. 6, line 67 - col. 7, line 2) do not anticipate the claimed management system and intelligent switches that use the destination identifier to

forward data (claims 9, 26) and use an algorithm to connect memory sections to communication channels (claim 17), among other things. Claims 12 and 29 recite, among other things, a temporary storage device that stores data to be written to a memory device, which the Examiner contends the claimed temporary storage device is taught by RAM 36 in BIU 16. (Office Action at 11). This is an incorrect contention because the Examiner also contends that the claimed memory device is also taught by RAM 36 in BIU 16. (Office Action at 8). Obviously, RAM 36 does not temporarily store data to be written to RAM 36, or perform all the other functions recited in these claims, as the Examiner contends.

For at least these additional reasons, *Ulug* fails to disclose each and every element recited in claims 9, 12, 17, 26, and 29 and therefore these claims are allowable over *Ulug*. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

35 U.S.C. § 102(b) Rejection of Claims 31-36

Claim 31, as amended, recites, among other things, a switch comprising a configurable switching fabric configured to form a connection between the memory section and a device external to the storage hub, wherein the switch directs data transferring between the memory section and the device across the connection because of destination information specifying the device. *Ulug* fails to teach each and every element recited in this claim.

As noted above, *Ulug* discloses simple switches controlled by a signal from a microprocessor indicating whether the BIU is in passive mode, active mode, or preemptive mode. (E.g., col. 5, lines 26-32; col. 6, line 67 - col. 7, line 2; col. 7, lines 29-

47). The microprocessor sends the signal according to a computer program that determines mode based on whether a packet is arriving on the bus, the priority of the packet, and when the packet has been processed by the BIU. (Col. 7, lines 42-47; Figs. 4-10 and accompanying text). *Ulug*'s switches do not "direct data transferring between the memory section and the device across the connection because of destination information specifying the device" as recited in claim 31 because they are set based on the arrival of a packet and the packet's priority. *Ulug*'s BIU does not consider destination information specifying a device external to the storage hub in determining how to set the BIU's switches.

For at least the foregoing reasons, *Ulug* fails to disclose each and every element recited in independent claim 31, and therefore claim 31 is allowable over *Ulug*. Dependent claims 32-36 are similarly allowable at least by reason of their dependence from allowable independent claims 31. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

The dependent claims are also allowable for additional reasons. For example, dependent claim 35 recites, among other things, a processor that substitutes a new address for the read address and forwards the new address to the memory section, causing data to be read from the memory according to the new address. The Examiner contends the claimed processor performing the recited functions is taught by microprocessors 22 and 50 in BIU 16. (Office Action at 11). This is an incorrect contention because microprocessors 22 and 50 do not substitute a new address for the read address and forward the new address to the memory section, causing data to be read from the memory according to the new address. Ulug lacks any disclosure

whatsoever regarding such functions, and the Examiner's contention that "as the next packet is different, the address will have to change" is a nonsequitor.

For at least these additional reasons, *Ulug* fails to disclose each and every element recited in claim 35 and therefore this claims is allowable over *Ulug*. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejection of claim 35.

35 U.S.C. § 103(a) Rejections

In the Office Action, the Examiner rejected claims 10, 11, 18, 19, 27, 28, and 32 under 35 U.S.C. § 103(a) as being unpatentable over *Ulug* in view of the Examiner's official notice of adding non-volatile RAM, memory fault detection and memory data block subject matter allegedly known in the art. Applicants traverse.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, the Examiner must demonstrate that (1) *Ulug* and the officially noticed subject matter disclose or suggest each and every limitation recited in the claims; (2) there is a reasonable probability of success of any modification of the teachings of *Ulug* with the officially noticed subject matter, and (3) there exists some suggestion or motivation, either in the teachings of *Ulug* itself or in the knowledge generally available to one of ordinary skill in the art, to make such a modification in a manner resulting in the claimed invention. *See* M.P.E.P. § 2143 (7th ed. 1998). Furthermore, each of these requirements must be found in the prior art – not based on Applicants' own disclosure. *See id.*

For the reasons detailed above, *Ulug* fails to teach or suggest several elements recited in independent claims 1, 14, 20, and 31, from which claims 10, 11, 18, 19, 27,

28, and 32 depend. Even assuming, *arguendo*, that the Examiner's official notice of non-volatile RAM, memory fault detection and memory data block subject matter allegedly known in the art is accurate, the official notice fails to teach or suggest the elements recited in claims 1, 14, 20, and 31 that are missing from *Ulug.* Accordingly, because *Ulug* combined with the Examiner's official notice fails to disclose each and every element recited in the base claims, dependent claims 10, 11, 18, 19, 27, 28, and 32 are allowable at least by virtue of their dependence from allowable claims 1, 14, 20, and 31.

In addition, with regard to claim 32, Applicants traverse the Examiner's official notice contention that non-volatile memory has advantages over volatile RAM in the context of *Ulug*'s BIU. First, the Examiner's reasoning is based on the false premise that "[t]he difference between the claim and *Ulug* is using a non-volatile memory instead of the volatile RAM." (Office Action at 13). This is incorrect because claim 32 recites the storage hub of claim 31 further comprising a non-volatile storage device. The non-volatile storage device is in addition to the memory section, not instead of it.

Second, as the Examiner seems to acknowledge, non-volatile memory may have advantages over volatile RAM, or it may not, "depending on the use requirements." (Office Action at 13). To support the rejection, the Examiner seeks to combine non-volatile memory with *Ulug*'s BIU to result in the claimed invention. Even if *Ulug* taught the elements of the base claim 31 (which it does not), there is no reasonable probability of success in modifying *Ulug* with non-volatile memory because non-volatile memory is too slow (i.e., it requires too long to read or write data) for use in a BIU. *Ulug's* BIU must be able to quickly read and write from RAM 36 in order to pass transient packets

down the bus to their destination at the bus speed. (E.g., col 7, lines 9-40). Applicants submit that non-volatile memory, especially the non-volatile memory available at the time that the present application was filed, has access times too slow to function in *Ulug*'s BIU. Furthermore, knowing the characteristic slow access speed of non-volatile memory, one of ordinary skill would have no motivation to modify *Ulug*'s BIU with non-volatile memory to result in the claimed invention. Instead, one of ordinary skill would be motivated not to make such a modification, as it would adversely affect the BIU's performance.

Accordingly, Applicants submit that there was no common knowledge in the art regarding replacing RAM with non-volatile memory given the use requirements of a BIU and request the withdrawal of the section 103 rejection of claim 32. Should the Examiner persist, Applicants request that the Examiner provide documentary evidence in the next Office Action that non-volatile memory can be used, and has advantages over volatile RAM, in a BIU, which is the device that the Examiner seeks to modify in a manner resulting in the claimed invention. (M.P.E.P. 2144.03).

Similarly, regarding claims 10, 18, and 27, Applicants traverse the Examiner's official notice contention that testing memory devices for faults and loading a back-up copy for fault recover is well known and beneficial in the context of *Ulug*'s BIU. As noted above, *Ulug*'s BIU must quickly read data from and write data into RAM 36 in order to service the high-speed bus traffic. Applicants submit that *Ulug*'s BIU could not provide test data to the RAM, receive the test data from the RAM, checking the received data, and determine a fault based on the checking of the test data and also use the RAM to service the bus traffic. These are functions performed by data storage systems,

not BIUs as the Examiner asserts. Even if *Ulug* taught the elements of the base claim 31 (which it does not), there is no reasonable probability of success in modifying *Ulug* with a memory test and fault recovery capability because it would slow the BIU down too much for it to perform its primary function of servicing bus traffic. Furthermore, knowing that slowing down a BIU would be detrimental to its primary function, one of ordinary skill would have no motivation to modify *Ulug*'s BIU by adding memory fault detection and recovery functions and devices to result in the claimed invention.

Accordingly, Applicants submit that there was no common knowledge in the art regarding adding memory test and fault recovery capability to a BIU in light of the speed requirements of a BIU and request the withdrawal of the section 103 rejection of claims 10, 18, and 27. Should the Examiner persist, Applicants request that the Examiner provide documentary evidence in the next Office Action that memory test and fault recovery capabilities can be used, and have advantages, in a BIU. (M.P.E.P. 2144.03).

Finally, regarding claims 11, 19, and 28, Applicants traverse the Examiner's official notice contention that using set associative memory has certain advantages over fully associative memory that are well known and beneficial in the context of *Ulug*'s BIU. Applicants submit that set associative memory would be detrimental in the context of *Ulug*'s BIU because, as *Ulug* teaches, the BIU operates on the basis of prioritized queues of information packets. (E.g., col. 6, lines 41-66). Because the BIU accesses the packets in the queue sequentially, one packet at a time, Applicants submit that there would be no advantages to using set associative memory in *Ulug*'s BIU. In fact, logic indicates that it would be disadvantageous to have to read or write an entire block of data out of a set-associative RAM 36, in order to access a single packet of data in the

block because it would take longer to access the entire block and separate out the desired packet than to just access the single desired packet from the queue using a fully associative memory. Further, even if *Ulug* taught the elements of the base claim 31 (which it does not), there is no reasonable probability of success in modifying *Ulug* with a set associative memory because it would slow the BIU down, impeding its ability to perform its primary function of servicing bus traffic. Further still, knowing that slowing down a BIU would be detrimental to its primary function, one of ordinary skill would have no motivation to modify *Ulug*'s BIU with set associative memory to result in the claimed invention.

Accordingly, Applicants submit that there was no common knowledge in the art regarding using set associative memory in *Ulug*'s BIU in light of the speed requirements of a BIU and the prioritized queue-based operation of the BIU, and request the withdrawal of the section 103 rejection of claims 11, 19, and 28. Should the Examiner persist, Applicants request that the Examiner provide documentary evidence in the next Office Action that using set associative memory is feasible, and has advantages, <u>in a BIU</u>. (M.P.E.P. 2144.03).

<u>Conclusion</u>

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: September 25, 2006

By: William J. Brogan
William J. Brogan
Reg. No. 43,515

EXHIBIT 12

PATENT
Customer No. 22,852
Attorney Docket No. 08812.0004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
Melvin James BULLEN et al.	)	Group Art Unit: 2189
Application No.: 10/284,278	)	Examiner: Christian Chace
Filed: October 31, 2002	)	Confirmation No.: 8809
For: METHODS AND SYSTEMS FOR A STORAGE SYSTEM WITH A PROGRAM-CONTROLLED SWITCH FOR ROUTING DATA(as amended)	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY TO OFFICE ACTION

In reply to the Final Office Action mailed September 26, 2005, the period for response to which extends through February 26, 2006, with a two-month extension, please enter the Request for Continued Examination filed herewith and amend the above-identified application as follows:

Amendments to the Specification are included in this paper.

Amendments to the Claims are included in this paper.

Remarks/Arguments follow the amendment sections of this paper.

02/27/2006 LWONDIM1 00000108 10284278

01 FC:1202 50.00 OP
02 FC:1201 200.00 OP

AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph 057 on page 16 with a corrected paragraph as follows:

Figure 3 illustrates a logical architecture for a management complex 26, in accordance with methods and systems provided. As illustrated, the management complex 26 may include functions that manage administrative ~~processes~~ processor 32 and functions that manage control ~~processes~~ processor 34. These management functions can include one or more central processing units (CPUs) for executing their respective processes. Additionally, the management complex 26 may use one or more application program interfaces (APIs) for communications between these functions.

Please replace paragraph 0128 on page 45 with a corrected paragraph as follows:

When the memory device 66 becomes available, the memory device 66 signals the microprocessor 51 in the section controller 54 via the memory section control circuitry 55. (Step [[1230]] 1228). This may, for example, be accomplished by the memory device 66 sending an interrupt signal to the microprocessor 51 via the memory device control circuitry 55. Then, the microprocessor 51 sends a message to the memory device 66 through the memory device control circuitry 55 to ready itself for storing the data (Step 1232). When the memory device is ready, the temporary storage memory interface device 60 passes the data to the T-selector 62, which, because this is a write operation, passes the data to the memory interface device [[60]] 64. For example, if the memory device 66 were available at Step [[1222]] 1224, the data need

not be stored in the temporary memory storage device 58. The data is then clocked into the shift register array 76 of the first memory interface device 64-1 where it is clocked through the write chain of shift register arrays 76 until it is loaded into the memory interface device 64 corresponding to the memory device 66 to which the data is to be written (Step 1234). The data is then written to the memory device at an address supplied by the section controller 54 of the memory section 30 (Step 1236).

Please replace paragraph 0137 on page 49 with a corrected paragraph as follows:

If the requested data block is not stored in the memory section 30, the section controller 54 sends a negative acknowledgement (NAK) message (Step 1314), through the CCI 46 and switch 22 to the requesting server 12. After receiving the NAK (Step 1316), the requesting server 12 may attempt to re-read (Step 1318) the data block from the memory section, may attempt to read the ~~device~~ data block from another device (not shown), or may inform the application. If the section controller 54 verifies that the memory section stores the requested data block, the microprocessor 51 in the section controller 54 determines which memory device 66 stores the data and checks its state to determine if the memory device 66 is busy or available (Step 1320). For example, as discussed above, the microprocessor 52 may store in its internal memory 52 a status code for each memory device 66 in the memory section 30 that the microprocessor 51 may consult to determine the availability of the memory device 66.

Please replace paragraph 0142 on page 51 with a corrected paragraph as follows:

If the memory device 66 at step [[10]] 1320 was busy, the read request may be queued in the internal memory 52 of the microprocessor 51 (Step 1322). When the memory device becomes available, it may send an interrupt signal to the section controller 54 (Step 1324), which then executes the read request as described beginning at Step 1326.

Please replace paragraph 0150 on page 55 with a corrected paragraph as follows:

In this example, so long as the requested data are resident in different memory devices 66, the memory section 30 itself may support N simultaneous reads and one write, where N is the number of communications channel connections available to the memory section 30 and preferably does not exceed the number of memory devices 66. For example, as illustrated in Figure 5, the communications channel interface 46 has 4 communications channels connections for transmitting and receiving information. The switch 22 preferably can handle simultaneous read requests and write requests that it can fulfill. The section controller 54 of the memory section 30 preferably manages the reading and writing of data to the memory devices 66 and manages any conflicts. The section controller 54 of the memory section 30 manages conflicts through the capabilities present in the software it executes. For example, the section controller 54 may direct that write requests have a priority higher than read requests with the lower priority requests being queued. For example, as previously discussed, the data for write

requests may be queued in the temporary storage device 58, and that write and read requests may be queued in the internal memory 52 of the section controller 54. The management complex 26 may direct the section controller 54 to resolve conflicts using other methods such as, for example, a first-to-arrive/a-first-to-be-processed algorithm.

Please replace paragraph 0162 on page 61 with a corrected paragraph as follows:

The signal is then passed to the read selector [[76]] 70 of the first memory interface device 64-1 (in this example) in the chain. Because, this is a write operation, the data is clocked into the shift register array 78 and is clocked through the shift registers until it is loaded into the shift register array 78 corresponding to the memory device 66 to which the data is to be written. The data is then written to the memory device 66. Methods and systems for writing data from a shift register array 78 to a memory device 66 are presented in more detail below.

Please replace paragraph 0163 on page 61 with a corrected paragraph as follows:

An exemplary reading operation for the embodiment of Figure 15 will now be described. First, an identifier (e.g., destination address, data block identifier, etc.) for the data is supplied to the read selector 84 from the section controller 54. The ~~destination address~~ identifier is then clocked through the chain of shift register arrays.

Please replace paragraph 0176 on page 66 with a corrected paragraph as follows:

The following provides a brief overview of an example for a reading operation for the memory section of Figure [[14]] 16. In this example, the communications channel interfaces 46 are preferably fibre channel I/O components. When a data request arrives at the communications channel interface 46, the communication channel interface 46 detects it and sends an interrupt signal to the section controller 54. This interrupt signal preferably includes information regarding the data block to be read from the memory devices. The section controller 54 then maps this data block information to an address in the memory devices. That is, the section controller determines from this data block information the memory devices 66 storing the requested data along with the addresses for this data on those memory devices. The section controller 54 then loads this address information into its internal memory, such that the addresses are transferred to the memory devices as in the above-describe memory latching example.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A storage system comprising

one or more memory sections, including

one or more memory devices including storage locations for storing data, and

a memory section controller for providing addresses to the memory devices, the addresses identifying storage locations for a memory device,

wherein the memory devices use the provided addresses to perform a function selected from the set of reading out and writing data to/from the memory devices;

one or more switches for receiving a data request including a data block identifier and switching the data request based on the data block identifier to one or more of the memory sections, the data block identifier identifying a set of storage locations;

wherein the memory sections to which the data request was switched forward the received data block identifier to its memory section controller which maps the data block identifier to a set of addresses for the storage locations identified by the data block identifier, and provides the set of addresses to one or more of the memory section's memory devices.

2. (Original) The storage system of claim 1, further comprising

a management system for providing an algorithm to at least one of the one or more switches, wherein the switch executes the algorithm in switching the data request based on the data block identifier.

3. (Original) The storage system of claim 2, further comprising:

a management system capable of performing fault management in response to a fault being detected.

4. (Original) The storage system of claim 3, wherein the management system is capable of detecting a fault with regard to a memory section in response to not receiving a message from the memory section.

5. (Original) The storage system of claim 3, wherein one or more of the memory sections are capable of detecting a fault in the memory section.

6. (Original) The storage system of claim 3, wherein the management system includes:

one or more control processors for performing fault management; and

one or more administration processors for collecting statistical data from the one or more switches and the one or more memory sections.

7. (Original) The storage system of claim 1, further comprising:

a management system capable of instructing the storage system to store a backup of data stored by one or more of the memory sections into a non-volatile storage device connected to at least one of the switches, receiving a fault message from a memory section, and instructing the storage system to load the back-up of the memory section's data from the non-volatile storage device into a functioning memory section.

8. (Original) The storage system of claim 1, further comprising

an interface for connecting to an external management system such that configuration management may be performed through the external management system.

9. (Original) The storage system of claim 1, further comprising:

one or more memory interface devices for receiving from at least one of the memory devices data stored in the storage locations identified by the addresses, combining the data with an identifier for use in forwarding the requested data, and forwarding the data to one or more of the switches;

wherein the switches to which the data was forwarded switch the data using the identifier and forward the data to the destination device.

10. (Original) The storage system of claim 9, wherein the identifier for use in forwarding the requested data is an address for a device to which the data are to be forwarded.

11. (Original) The storage system of claim 9, wherein the identifier for use in forwarding the requested data is an identifier for identifying the data that are to be forwarded.

12. (Original) The storage system of claim 9, wherein the memory devices include outputs, and wherein at least one of the memory interface devices includes:

at least one set of shift registers interconnected in series, wherein at least one of the shift registers receives a clock signal having a shift frequency, and wherein the shift register is capable of shifting data loaded into the shift register to a next one of the shift registers in the set according to the shift frequency; and

wherein data from one or more of the output of a memory device is loaded into a corresponding shift register in the sets of shift registers and the loaded data is shifted from the shift register to a next one of the shift registers in the set according to the shift frequency, such that the shift register maintains its shift frequency during any loading of the data.

13. (Original) The storage system of claim 9, wherein the memory devices include outputs, and wherein at least one of the memory interface devices includes:

at least one set of shift registers interconnected in series, wherein at least one of the shift registers receives a clock signal having a shift frequency, and wherein the shift register is capable of shifting data loaded into the shift register to a next one of the shift registers in the set according to the shift frequency; and

wherein data in the set of shifted register is loaded according to the clock signal from one or more shift registers in the set into one or more of the memory devices via an input corresponding to the shift register, such that the shift register maintains its shift frequency during any loading of the data.

14. (Original) The storage system of claim 1, wherein at least one memory section further includes

a temporary storage device for storing data to be written to a memory device; and

a temporary storage interface device for storing data in and retrieving data from the temporary storage device;

wherein at least one of the switches is capable of, in response to receiving data to be stored in the memory section, forwarding the data to the temporary storage interface device, and wherein the temporary storage interface stores the data in the temporary storage device if a memory device to which the data is to be written is busy, and wherein the temporary storage interface device retrieves the data from the temporary storage device when the memory device is no longer busy and forwards the data to the memory device such that the memory device stores the data.

15. (Original) The storage system of claim 1, wherein at least one memory section further includes at least one communications channel interface for receiving data to be stored by the memory section and transferring the data to be stored to one or more of the memory devices, and wherein the communications channel interface is

further capable of receiving data read from the memory devices and transferring the data read from the memory devices to one or more of the switches, and wherein the communications channel interface is further capable of receiving data requests and forwarding the data requests to the memory section controller.

16. (Original) A method for use in a storage system, comprising:

storing data in storage locations in a memory device;

receiving by a switch a data request including a data block identifier;

the switch switching the data request based on the data block identifier to a memory section including the memory device, the data block identifier identifying a set of storage locations in the memory device;

forwarding the received data block identifier to a memory section controller;

the memory section controller mapping the data block identifier to a set of addresses for the storage locations identified by the data block identifier; and

the memory section controller providing the set of addresses to the memory device; and

the memory device using the provided addresses to perform a function selected from the set of reading and writing data to/from the memory device.

17. (Original) The method of claim 16, further comprising

a management system providing an algorithm to the switch; and

the switch executing the algorithm in switching the data request based on the data block identifier.

18. (Original) The method of claim 17, further comprising:

a management system performing fault management in response to a fault being detected.

19. (Original) The method of claim 18, further comprising:

the management system detecting a fault in response to not receiving a message from the memory section controller.

20. (Original) The method of claim 18, further comprising:

the memory section controller detecting a fault.

21. (Original) The method of claim 16, further comprising:

storing a back-up of data stored by the memory device into a non-volatile storage device connected to the switch;

a management system receiving a fault message from the memory section controller; and

the management system instructing the non-volatile storage device to send the back-up of the memory device's data to a functioning memory device.

22. (Original) The method of claim 16, further comprising:

a memory interface device receiving from the memory device data stored in the storage locations identified by the addresses;

the memory interface device combining the data with an identifier for use in forwarding the requested data;

the memory interface device forwarding the data to the switch;

the switch switching the data using the identifier; and

the switch forwarding the data to a destination device.

23. (Original) The method of claim 16, further comprising:

a memory interface device in the memory section receiving, in response to the memory section receiving a data request, data from a memory device;

shifting data in one or more shift registers in a set of shift registers interconnected in series from the shift register to a next one of the shift registers in the set on the basis of a clock signal having a shift frequency, wherein the shift registers are included in the memory interface device;

loading data from the memory device into a corresponding shift register in the set; and

shifting the data loaded into one or more of the shift registers to a next one of the shift registers in the set according to the clock signal, wherein the shift register maintains its shift frequency during the loading of the data from the memory devices into the shift registers.

24. (Original) The method of claim 16, further comprising:

a memory interface device in the memory section receiving, in response to the memory section receiving a data request, data from a memory device;

shifting data in one or more shift registers in a set of shift registers interconnected in series from the shift registers to a next one of the shift registers in the set on the basis of a clock signal having a shift frequency, the shift registers included in the memory interface device;

loading data from one or more of the shift registers to a memory device; and

shifting the data loaded from the one or more shift registers to a next one of the shift registers in the set according to the shift frequency after the data is loaded into the memory device, wherein the shift register maintains its shift frequency during the loading of the data.

25. (Original) The method of claim 16, further comprising:

the memory section receiving data to be stored in the memory device;

forwarding the data to a temporary storage interface device;

the temporary storage device storing the data in a temporary storage device if the memory device to which the data is to be written is busy;

the temporary storage interface device retrieving the data from the temporary storage device when the memory device to which the data is to be stored is no longer busy; and

the memory device storing the data.

26. (Original) A storage system, comprising:

means for storing, including:

forwarding

means for storing data in storage locations, the means for storing data in storage locations including means for reading data stored in the storage locations using an address;

means for controlling the means for storing, the means for controlling including:

means for controlling the means for storing, the means for controlling including:

means for mapping a data block identifier to a set of addresses,

means for providing the addresses to the means for storing data in storage locations, the addresses identifying storage locations;

means for switching, including

means for receiving a data request including a data block identifier;

means for switching the data request based on the data block identifier to a means for storing, the data block identifier identifying a set of storage locations in the means for storing data in storage locations; and

means for forwarding the received data block identifier to the means for storing.

27. (New) A storage hub comprising

a memory section, including

a memory device including storage locations for storing data, and

a memory section controller for providing an address to the memory device, the address identifying a storage location,

wherein the memory device uses the provided address to write data into the [redacted]ory device; and

a switch, comprising a configurable switch fabric, for receiving a data request including a data block identifier and transmitting the data request to the memory section determined by applying the data block identifier to an algorithm that configures the switch fabric, and for receiving write data associated with the data request and transmitting the write data to the determined memory section;

wherein the memory section forwards the received data block identifier to the memory section controller, which determines from the data block identifier the address of the storage location and provides the address to the memory device, and the memory device stores the write data at the address.

REMARKS

Applicants thank the Examiner for considering the IDS filed by Applicants on March 7, 2005, and for withdrawing the objections to the specification and title, withdrawing the rejection of claims 12 and 13 under the doctrine of obviousness-type double patenting in view of U.S. Patent No. 6,879,526, and withdrawing the rejection of claim 26 under 35 U.S.C. § 112, second paragraph.

In this Reply after Final, Applicants have amended the specification to correct minor typographical errors and added new claim 27. No new matter has been added. Claims 1-27 are pending.

Summary

In the final Office Action, the Examiner provisionally rejected claims 1, 2, 7, and 12-16 under the doctrine of obviousness-type double patenting in view of copending U.S. Application No. 10/284,268; rejected claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4, 796,231 to *Pinkham*; and rejected claims 3-7 and 18-20 under 35 U.S.C. § 103(a) as being unpatentable over *Pinkham* in view of the Examiner's official notice of memory fault detection and recovery techniques allegedly known in the art. For the reasons given below, Applicants traverse these rejections as currently understood, request the withdrawal of the finality of the Office Action mailed September 26, 2005, and request issuance of a new office action that fully and clearly states the ground of rejection for the claims of this application.

In the Office Action, the Examiner also incidentally alleged that U.S. Patent No. 4,510,599 to *Ulug* ("*Ulug*") and U.S. Patent No. 6,728,799 to Perner et al. ("*Pemer*") also anticipate claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b), but did not rely on *Ulug* or *Pemer* as a basis for rejection. Accordingly, Applicants need not address

the allegations based on these unasserted references, which would be unfounded in any case.

Double Patenting Rejection

In the Office Action, the Examiner provisionally rejected claims 1, 2, 7, and 12-16 under the doctrine of obviousness-type double patenting in view of copending U.S. Application No. 10/284,268. In accordance with M.P.E.P. §§ 804 and 1490, and without agreeing with the Examiner's allegations of anticipation and double patenting, and while reserving the right to traverse the Examiner's allegations of anticipation or double patenting in the future, Applicants defer responding to the provisional double patenting rejection until it is the only rejection remaining in the two applications, and the Examiner withdraws the provisional double-patenting rejection as to one application and permits that application to issue as a patent, thereby converting the provisional double patenting rejection in the other application into a double patenting rejection at the time the other application issues as a patent.

The Office Actions Do Not Fully and Clearly State the Grounds of Rejection Under 35 U.S.C. §§ 102 and 103

Because the pending final Office Action and the first Office Action mailed March 18, 2005, do not refer to the claims of this application, Applicants cannot accurately discern the Examiner's interpretation of the present claims, the Examiner's assertions as to how the cited reference allegedly teaches each feature of the present claims, or the Examiner's reasons for rejecting the present claims, among other things. "Where a claim is refused for any reason relating to the merits thereof it should be "rejected" and the ground of rejection fully and clearly stated . . . ." M.P.E.P. § 707.07(d). In both Office Actions for this application, the Examiner apparently used text cut and pasted

from the Office Actions for copending application 10/284,268 as the stated reasons for rejecting the claims of the present application. The cut-and-pasted text, however, refers to the features recited in the claims of copending application 10/284,268, and the words and features of those claims do not correspond to the words and features recited in the claims of the present application. Claim features stated in the cut-and-pasted text do not appear in the claims of the present application, and features claimed in the present application are not addressed in the cut-and-pasted text of the Office Actions. In addition, the Examiner has presented no reason at all for rejecting claim 21 in either Office Action. Consequently, the Examiner has not fully and clearly notified Applicants of the reasons for rejecting the claims of the present application, and Applicants are not being given a fair chance to address the rejections. Accordingly, Applicants request that any future office action meets the requirements of 37 C.F.R. §§ 1.104 and 1.113 and M.P.E.P. §§ 706 and 707.

The two Office Actions issued for this case do not meet the requirements of the Rules and the M.P.E.P. "The examiner's action will be complete as to all matters . . . ." 37 C.F.R. § 1.104(b). "The applicant . . . will be notified of the examiner's action. The reasons for any adverse action or any objection or requirement will be stated in an Office action and such information or references will be given as may be useful in aiding the applicant, or in the case of a reexamination proceeding the patent owner, to judge the propriety of continuing the prosecution. 37 C.F.R. § 1.104(a)(2). "In accordance with the patent statute, 'Whenever, on examination, any claim for a patent is rejected, or any objection . . . made,' notification of the reasons for rejection and/or objection together with such information and references as may be useful in judging the propriety

of continuing the prosecution (35 U.S.C. 132) should be given." M.P.E.P. § 707. The Office Actions mention the claim numbers of the present application but apply the cited reference to the recited claim features of copending application 10/284,268. This does not provide Applicants with full and clear reasons for the adverse action and is not useful in aiding Applicants in judging the propriety of continuing prosecution because the Office Actions do not address the features recited in the claims of the present application. Applicants need to know how and why the Examiner is applying the cited reference to the features recited in the claims of this application in order to formulate reasoned arguments or amendments. It is unfair to require Applicants to guess or infer the Examiner's reasons for rejection of the claims of this application by reading the Examiner's reasons for rejecting the claims of copending application 10/284,268.

Moreover, as the Examiner has not provided any reason for the rejection of claim 21, Applicants assume it is allowable over the art of record and request acknowledgment in the next office action.

Traversal of 35 U.S.C. § 102 Rejections

As in the previous Reply, to avoid an incomplete response Applicants will attempt to address what they believe to be the grounds for rejection of the pending claims under sections 102 and 103, although the Examiner's grounds are not clear from the statements in the Office Actions.

In the final Office Action, the Examiner maintained the rejection of claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4, 796,231 to Pinkham ("*Pinkham*"). For the reasons that follow, Applicants maintain the traversal of the rejection of claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(b).

In order to properly anticipate claims 1, 2, 8-17, and 20-26 under 35 U.S.C. § 102(a), *Pinkham* must be shown to explicitly disclose each and every limitation recited in the claims. *See* M.P.E.P. § 2131. If *Pinkham*, however, fails to expressly set forth a particular limitation, then the Examiner must show that this limitation is inherently disclosed to substantiate a claim of anticipation. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). To establish inherency, the Examiner must specifically identify extrinsic evidence that makes clear to one skilled in the art that the missing limitation "is necessarily present" in the *Pinkham* disclosure. *See id.; see also Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1269 (Fed. Cir. 1991).

Pinkham does not disclose each and every limitation recited in the claims, which include the functions, operations, connections, and interactions of the combinations of devices expressly recited in the claims.

For example, independent claim 1 recites, among other things, "one or more switches for receiving a data request including a data block identifier and switching the data request based on the data block identifier to one or more of the memory sections, the data block identifier identifying a set of storage locations."

For the reasons given in the last response (hereby incorporated herein by reference), Applicants maintain that *Pinkham* fails to teach this claim feature, among others.

In maintaining the section 102 rejection of claims 1, 2, 8-17, and 20-26, the Examiner contends that *Pinkham* discloses the claimed switches, control signals, and memory section controller because *Pinkham*'s switches "must, inherently, receive a control signal of some sort – how else would they know whether or not to switch?" and

because "the management system is inherently in place in *Pinkham* as different methods of operation (serial and cascaded) are used. Something has to tell the system which one to use – that would be the 'management system.'" (Office Action at 11).

Pinkham's own disclosure, however, reveals the answers to the Examiner's own questions by making clear that *Pinkham* does not teach an inherent management system and control signals for its "switches." There are no inherent management systems, no inherent control signals for switching, and no inherent controller for changing from serial to cascaded mode because *Pinkham*'s "switches" are not switches—they are merely a shorthand way to illustrate two different circuit design options that are chosen before implementation and hardwired into the circuit:

> Each of the switches 56-62 is a metal mask programmable option which is selected during fabrication of the semiconductor memory. Although illustrated as switches, they are in actuality a series of lines which are connected or disconnected on the mask prior to fabrication of the device.

(Col. 5, lines 58-64; see also col. 10, lines 57-60, col. 17, lines 11-14).

Thus, *Pinkham's* "switches" do not and cannot switch and consequently do not inherently receive a control signal from an inherent management system as the Examiner contends.

Moreover, as explained in the last response, even if there were a management system that sends control signals to the "switches" disclosed by *Pinkham* (which there is not), the simple single pole double throw switches illustrated in *Pinkham* do not anticipate the claimed management system or intelligent switches that receive a data request including a data block identifier (claims 1, 16) execute an algorithm to switch the data request based on the data block identifier (claims 2, 17), switch forwarded data using an identifier and forward the data to a destination device (claim 9), etc. Contrary

to the Examiner's contention that "the claims do not require a specific method of use of the identifier," claim 1, for example, does expressly require that the switch 1) "receiv[e] a data request including a data block identifier," and 2) "switch[] the data request based on the data block identifier to one or more of the memory sections." The claimed functionality is not taught by a single pole double throw switch because it has no processor or other means to "receive a data request" or "execute an algorithm," and *Pinkham* fails to disclose any other switching devices with such functionality.

For at least these reasons, *Pinkham* fails to disclose each and every element recited in claims 1, 16, and 26 and therefore these claims are allowable over *Pinkham*. Claims 2-15 and 17-25 are allowable at least by reason of depending from an allowable base claim. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

As explained in the last response, dependent claims 12, 13, 23, and 24 are also allowable for at least one additional reason. Applicants maintain that *Pinkham* does not teach or suggest, among other things, "that the shift register maintains its shift frequency during any loading of the data," as recited in claims 12, 13, 23, and 24 because *Pinkham* discloses conventional shift registers 34-40 that cannot load data to and from the memory arrays 10-16 while continuing to shift according to their shift frequency.

In maintaining the section 102 rejection of claims 12, 13, 23, and 24, the Examiner contends that:

> The shift frequency is the clock frequency going into the shift register. The frequency of that clock does not change, whether or not data is loaded or shifted or both. The claim does not require that data is actually shifted at the same time it is loaded.

Applicants submit that the Examiner is misinterpreting the claim language. Although the Examiner has interpreted "shift frequency" in the claims as referring to the frequency of the clock whose signals control the shift register, in claims 12, 13, 23, and 24, "shift frequency" refers to the frequency at which the shift register itself shifts, not the frequency of the clock. For example, claim 23 expressly recites "that the shift register maintains its shift frequency during the loading of the data from the memory devices into the shift registers." (Emphasis added).

For at least these additional reasons, Applicants maintain that *Pinkham* fails to disclose each and every element recited in claims 12, 13, 23, and 24, and therefore these claims are allowable over *Pinkham*. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

As explained in the last response, claims 9, 10, and 22, are also allowable for at least one additional reason. Applicants maintain that *Pinkham* does not teach or suggest "an identifier for use in forwarding the requested data," as recited in claims 9, 10, and 22.

In maintaining the section 102 rejection of claims 9, 10, and 22, the Examiner stated that Applicants' arguments are not commensurate with the scope of these claims. To the contrary, Applicants submit that it is the Examiner's unreasonable broad interpretation that is not commensurate with the scope of both these claims and all the other pending claims. During examination, the claims must be interpreted as broadly as their terms reasonably allow consistent with the specification, and the words of the claims should be given their plain meaning. M.P.E.P. § 2111.01 (8th ed., May 2004 rev.) (citing *In re American Academy of Science Tech Center*, 367 F.3d 1359 (Fed. Cir.

2004) and *In re Zietz,* 893 F.2d 319, 321 (Fed. Cir. 1989)). To the best of Applicants' understanding from the Office Actions, the Examiner interprets "an identifier for use in forwarding the requested data" so broadly that *Pinkham's* address A0-A7 when used for reading data from memory arrays 10-16 is said to anticipate the claimed combination of features, including an identifier for forwarding the requested data. Applicants respectfully submit that the Examiner's interpretation is unreasonably broad because it is inconsistent with the usage in the specification, inconsistent with the rest of the claim language, and contrary to the ordinary meaning of the term in the art. *Id.* Claim 9, for example, expressly recites that "the switches to which the data was forwarded switch the data using the identifier," but nothing in *Pinkham* (e.g., switches 56-62) switch using read address A0-A7 because there is no switching device connected to the address lines A0-A7 or address decoder for address A0-A7. Moreover, even using, *arguendo*, the Examiner's overly broad interpretation, *Pinkham* does not teach or suggest that "the identifier for use in forwarding the requested data is an address for a device to which the data are to be forwarded" as recited in claim 10 because A0-A7 is a data address in memory arrays 10-16, not the address of another device. Therefore, *Pinkham* cannot anticipate the claimed combination of elements recited in claim 10. To interpret claim 10 otherwise contradicts the plain meaning of the words of the claim. Similarly , *Pinkham* does not teach or suggest a "memory interface device combining the data with an identifier for use in forwarding the requested data," and "the switch switching the data using the identifier" as recited in claim 22 because *Pinkham's* address lines A0-A7 and address latches 20, 22 and decoder 30, 52 are not connected to the data output of the memory arrays 10-16. Therefore, *Pinkham* cannot anticipate the claimed

combination of elements recited in claim 22. The Examiner's interpretation is unreasonable because it is irreconcilable with the plain meaning of the words of claim 22.

For at least these additional reasons, Applicants maintain that *Pinkham* fails to disclose each and every element recited in claims 9, 10, and 22, and therefore these claims are allowable over *Pinkham*. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Other features recited in dependent claims are also not disclosed by Pinkham, but it is difficult to point them all out because of the lack of specificity of the Office Actions. Examples include "a temporary storage device for storing data to be written to a memory device . . . wherein at least one of the switches is capable of, in response to receiving data to be stored in the memory section, forwarding the data to the temporary storage interface device, and wherein the temporary storage interface stores the data in the temporary storage device if a memory device to which the data is to be written is busy, and wherein the temporary storage interface device retrieves the data from the temporary storage device when the memory device is no longer busy and forwards the data to the memory device such that the memory device stores the data" as recited in claims 14 and 25. Pinkham's I/O buffer 66, which the Examiner contends anticipates these claims, is used to hold data that may be blocked by a write mask that controls which memory arrays 10-16 may be written to. As shown in Figure 1 of Pinkham and explained at column 16, line 29 through column 17, line 27, I/O buffer 66 is not connected to "switches" 56-62, (which the Examiner contends anticipate the claimed switches). Therefore, I/O buffer 66 cannot and does not perform the functions of the

temporary storage device and switches recited in claims 14 and 25, and *Pinkham* cannot anticipate the combination of features recited in the claims.

Similarly, Pinkham's I/O buffer 66 does not anticipate the "communications channel interface" recited in claim 15, because without a connection to Pinkham's switches, I/O buffer 66 cannot and does not "transfer[] the data read from the memory devices to one or more of the switches." Nor does I/O buffer 66 have any function or connection related to "receiving data requests and forwarding the data requests to the memory section controller" as recited in claim 15. Accordingly, *Pinkham* cannot anticipate the combination of features recited in this claim.

For at least these additional reasons, Applicants maintain that *Pinkham* fails to disclose each and every element recited in claims 14, 15, and 25, and therefore these claims are allowable over *Pinkham*. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 102 rejections of all these claims.

Traversal of 35 U.S.C. § 103 Rejections of Claims 3-7 and 18-20

For the reasons given in the previous response, the Office Actions fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 at least because *Pinkham* and the officially noticed techniques do not disclose or suggest each and every limitation recited in the claims. As explained above, *Pinkham* fails to teach or suggest several elements recited in independent claims 1, 2, 16, and 17, from which claims 3-7 and 18-20 depend. Accordingly, because *Pinkham* combined with the Examiner's official notice of allegedly known subject matter fails to disclose each and every element recited in the base claims, dependent claims 3-7 and 18-20 are allowable at least by virtue of their dependence from allowable base claims.

Conclusion

In view of the foregoing remarks, Applicants respectfully request reconsideration and reexamination of this application, the withdrawal of the finality of the Office Action mailed September 26, 2005, the issuance of a new office action that fully and clearly states the ground of rejection for the claims of this application, including claim 21, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: February 24, 2006

By: William J. Brogan
William J. Brogan
Reg. No. 43,515